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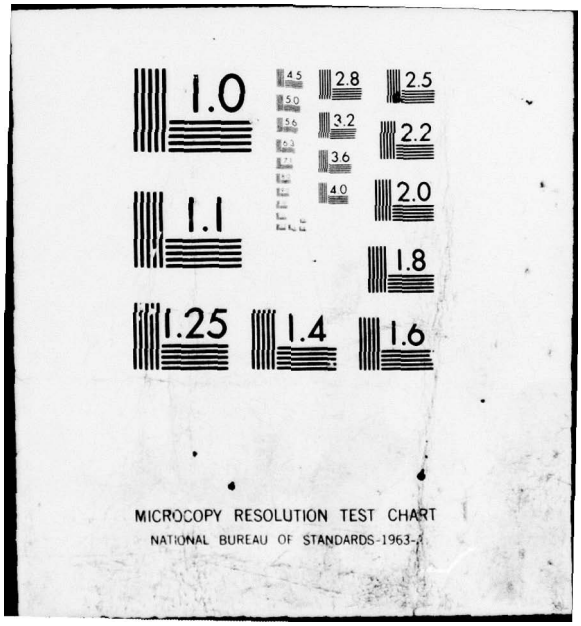
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GaAs ANALOG INTEGRATED CIRCUITS (GaAs RF-LSI)

PHASE I PROGRESS REPORT

VOLUME I. TECHNICAL

August 1979

Contract No. N00039-78-C-0305

Prepared for
NAVAL ELECTRONIC SYSTEMS COMMAND
AND NAVAL RESEARCH LABORATORY
Washington, D.C.

By

TRW
DEFENSE AND SPACE SYSTEMS GROUP
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PHASE I. PROGRESS REPORT.

VOLUME I. TECHNICAL.

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(11) Aug [redacted] 79

(9) Rept. for 5 Jun 78 - 5 Jun 79.

(15) Contract No. N00039-78-C-0305

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CONTENTS

1. INTRODUCTION AND SUMMARY

This preliminary technical progress report describes the results of the first phase of the GaAs RF-LSI Development Program, Contract No. N00039-78-C-0305, performed for the Naval Electronic Systems Command (code ELEX3042) by TRW Defense and Space Systems Group. The period of performance for the first phase activities is 5 June 1978 to 5 June 1979. The overall objective of the GaAs RF-LSI Development Program is the development of a family of monolithic GaAs analog integrated circuits operating at frequencies through X-band, and the implementation of a monolithic X-band receiver which combines a number of these building block circuits. The aim of the first phase effort was to amass the analysis, design, and process technology tools with which to implement the building block circuits and later the receiver.

The general objective of Phase I, Device, Process and Circuit Techniques Investigation, was to undertake the device and process technology development necessary to support the Phase II, MSI Building Block Development. Closely coupled with the actual process development were theoretical studies addressing optimization of devices and circuit techniques for monolithic implementation. The following is a brief task by task summary of the work accomplsihed. The sections which follow this introduction are expanded discussions of each of the tasks.

1.1 PROCESS RELATED DEVICE MODELS

The objective of this task was to provide process related small signal and noise models for the two principal active GaAs devices, the planar gate-controlled transferred electron logic devices (TEDs), and the field effect transistor (FETs). As it happened, between the time the original proposal for this program was submitted and the actual program start, opportunities arose to get a very substantial headstart on this task. Through a combination of contract and internally funded efforts, basic model type selection was made for both the TEDs and FETs, the governing equations were placed into computer program and tested, device optimization routines were added, and provisions for calculating dc current-voltage relations were incorporated. Thus, at contract start, work on the device models had already been underway for about nine months. That work, coupled with the model development work supported by this program and subsequent internally funded efforts, have produced models which are much more sophisticated and complete than would otherwise have been possible.

The TED model was begun by establishing the field conditions which must exist within the device to a) prevent spurious device outputs when a logic "0" signal is applied to the input gate, and to b) provide high sensitivity (i.e., a high probability of triggering a device output) to a logic "1" input. Prior to the program start, a TED model was developed, which, for a single input gate device, would optimize doping concentration

(n_o), channel thickness (a), gate length (l_g), cathode-anode bias (V_{ca}), and gate bias (V_{gc}), while minimizing dc power and providing good noise immunity. This single gate device is only used as either a threshold detector or frequency divider, and represents the simplest case of a TED logic device.

The TEDs planned for use in this program require at least two input gates, and four gates is the most complex case of practical interest. Therefore, during this program the TED model was generalized to treat one through four-gate TEDs, and to predict not only the optimum device design and bias conditions, but also to provide a multidimensional map of the ranges of n_o, a, lg, V_{ca}, and V_{gc} over which the desired logic functions can be realized.

The FET model development began with a literature search to determine which of the several available models was best suited to the purposes of process related device design for integrated circuit applications. The FET model, which offered the fewest restrictions and which was best derived from basic physical properties, is generally known as the "Pucel model" (for references see the end of Appendix A). This model was programmed and tested as it appears in the literature with some minor corrections reflecting more recent research in the areas of electron temperature as a function of field and the low field mobility dependence on doping concentration. After the initial testing of the model had shown good correlation with published noise figure data, optimization routines were added to allow individual analysis of the effects of the intrinsic region (the region under the gate) and the ancillary regions on noise figure performance, transconductance, and cutoff frequency. This work was completed just prior to the contract start, and essentially comprised a FET noise model. Given that the model was in a more advanced state than expected at the program start, we have been able, during the program, to develop a much more sophisticated model than was originally proposed.

The contract work which was performed on the FET model is summarized below:

- S-parameter calculations were added, as were gain calculations from the S-parameters
- The program was extensively rewritten to be interactive and to run on the timesharing system rather than in batch mode.
- An improved expression for electron temperature as a function of device temperature and electric field was developed.
- A fairly extensive subprogram was developed which permits a two-dimensional analysis of devices with any vertical doping profile which can be described either analytically or by a table. This was verified with Rockwell data via private communications.
- The simplifying assumptions in Pucel's work which restricted analysis to devices with gate length (L) to epi thickness (a) ratios greater than three were removed. All output functions are well behaved for L/a ratios as small as one, and experimental verification has been obtained for L/a ratios as small as two.

- Extensive comparisons were made throughout between measurement data and computer predicted data. Measurement data was obtained both from the literature and from our own labs on both TRW devices and purchased devices.

Correlations achieved between device data and predicted data have been quite good. The subjects of greatest import to the planned IC development are predictions of dc IV characteristics and either the S-parameters or the element values for the equivalent circuit model. The dc IV characteristics must be known so that one can set up proper biasing internal to the circuits. The S-parameters or equivalent circuit element values are essential to the RF circuit design process. Measurement vs prediction data for the S-parameters and IV characteristics is given in Section 2.

A third feature of the FET model, noise figure prediction, has been the subject of some controversy for the past several months. For FETs of conventional design, the model predicts results which are quite consistent with measurement data for gate lengths of from 0.5 to 2.0 microns. The model also predicts that significant noise figure reduction could be achieved by ion implanting the regions outside the gate area to a doping concentration much higher than that used in conventional designs, and using a concentration under the gate of about half the usual level. The controversial aspects of this result have to do both with the amount of improvement obtainable and with the rather steep slope of noise figure as a function of gate area doping concentration. Other models, Fukui's for example, predict a similar trend of lower noise figures associated with lower gate doping concentration, but none show as strong a dependence as TRW's model. At the time the contract work on the FET model was ended, this somewhat surprising result was left unresolved.

TRW has continued and is continuing to improve the FET model; this work will no doubt go on for as long as FET devices and ICs are of interest, just as work continues in a number of places at improving upon bipolar transistor models. Specifically, since the contract work was completed, an updated diffusion constant relationship and expressions for the interelectrode parasitic capacitances and capacitances associated with the bonding pad areas have been added. These have had the effect of bringing the phase angles associated with the input and output reflection coefficients, S_{11} and S_{22}, to even better agreement. Further, the addition of these capacitances reduces the slope of the noise figure vs doping concentration curves to be similar to the Fukui model predictions, and increases the predicted minimum noise figure to a more "reasonable" value.

While it was recognized earlier that the controversial result of the strong noise figure vs doping concentration dependence could have been made less so, we declined to do this artifically, that is without a sound physical justification. The additions of the parasitic capacitances particularly apply to discrete devices in which the contact areas and pads are much larger than they would be for IC devices, and one can conclude that there is some noise figure penality associated with the practical requirement for

these bonding pads. We are still not fully satisfied with our modeling of the diffusion constant term, although our model is consistent with the most recent published results. This matter is being further researched. The model's prediction of significant noise figure improvement at low temperatures (77°K is optimal) has been experimentally verified. Data is given in Section 2.

1.2 INTEGRATED CIRCUIT MODELS

The second program task originally called for incorporation of the device models into SPICE, a commercially available circuit analysis program. It was recognized as this task began that it would also be very useful to incorporate the FET model into COMPACT, and this was done as well.

SPICE has four basic options which are used in circuit design in conjunction with the device models: small signal analysis, large signal analysis, transient response analysis and Fourier analysis. The device models are incorporated into SPICE for small signal (steady state) and transient analysis by means of a data record which is essentially a listing of the model equivalent circuit element values. These are then embedded into a proposed circuit (say an amplifier or oscillator), and the program analyzes the circuit performance. For typical amplifier designs, the basic response is determined from SPICE's small signal analysis, and then the circuit is tested for potential instabilities via the transient analysis. Oscillator design is carried out primarily via the transient analysis reotines which inject a starting pulse (simulating noise) into an oscillator circuit and then examine the time domain response to dertermine the oscillation frequency and amplitude.

There are certain circuits, those involving frequency conversion of which analog multipliers are a prime example, which must be analyzed by the large signal model and the Fourier analysis routine. For these cases we made minor modifications of SPICE's JFET model to adapt it to MESFET circuit analysis. TRW's FET model includes as one of its options a large signal output. However, we have found this to be somewhat cumbersome for use with SPICE, and have developed some simpler expressions for SPICE analysis. The analog multiplier designs described in Section 5.3 provide examples of SPICE used in this mode.

COMPACT is a commercial CAD program which differs from SPICE in two key ways. Firstly, it accepts device S-parameters as inputs rather than equivalent circuit element values. Secondly, it contains optimization routines which allow one to select a circuit topology and starting values for the circuit elements and have COMPACT optimize those element values for desired circuit performance. Since COMPACT works with device S-parameters, one can input directly measured data rather than equivalent circuit element values which must be derived from either the device models or from device measurement data. An example of a COMPACT circuit design is given in Section 5.2.

In addition to circuit design with COMPACT, it is also used for analysis of device design and performance, and model testing in the following way. Suppose a device has been fabricated and characterized. Its measured S-parameters as a function of frequency are input to COMPACT and COMPACT provides the best fit element values for the FET equivalent circuit model, and a printout of the new S-parameters calculated from that model. The device's physical characteristics (n_0, a, Lg, etc.) are entered into the FET model program which also predicts the equivalent circuit model and S-parameters. If the COMPACT and FET model outputs are a good fit, the analysis is done. If not, one returns to the device model and adjusts input parameters until a good fit is achieved. By this method feedback is provided to the device processors on quantitites like doping concentration as derived from device measurements to compare against measurements made on the unprocessed wafers. This method has also been used to compare published S-parameter results with those which would be predicted by our FET model.

1.3 PROCESS DEVELOPMENT

The real crux of the Phase I contract work is the development of several key processing technologies which will be required to implement the building block circuits and the monolithic receiver. During the first phase of the program, the major tasks were to:

- Develop a repeatable ion implanatation process for application to planar circuits
- Implement multi-implant technology for device improvements and for providing both TEDs and FETs in planar integrated circuits
- Implement processing techniques capable of yielding small geometry devices on large scale integrated circuits.

The thrust of this work is towards developing a fully planar implementation process for all-FET circuits (analog multiplier, amplifier, etc.) and for circuits which combine both FETs and TEDs (modulator and demodulator). Additional tasks included:

- Multiple ion implant for: FET active gate region, FET source and drain-to-gate region, and the ohmic contact regions. This included capping and annealing techniques.
- Employ epi growth and ion implantation techniques to optimize TEDs and FETs on a given wafer in a planar form.
- Fabricate devices using a FET and TED mask developed on this program. The mask set includes test vehicles for IC studies.
- Develop a test mask with an experimental analog mutiplier. Fabricate devices using this mask and evaluate device models and circuit performance predictions.

The process development work is described in detail in Section 4. A brief summary of the key accomplishments follows:

- Developed a reliable substrate qualification technique

- Developed a repeatable ion implantation process including (a) the investigation of threee N-type dopant ions, (b) a reliable plasma nitride capping and annealing process
- Demonstrated multi-ion implant capability for device improvement—N+ for contacts and N-channel doping using Si+ ions
- Fabricated planar TEDs using boron isolation
- Developed improved metallization giving $R_s = 10^{-6} \Omega\text{-cm}^2$
- Improved photoresist lift technique giving 1 μm gate structures
- Fabricated over 40 wafers using existing masks to establish a repeatable ion implant process.

The repeatability of the ion implant process is evidenced by the small standard deviations measured on a series of 40 wafers of peak concentration of $1.6 \pm 0.4 \times 10^{17} \text{cm}^{-3}$ and depth of 0.24 ± 0.04 μm one order of magnitude below the peak concentration. This was successful only after developing a technique for qualifying wafers. With this qualification technique, 14 crystals from seven suppliers were investigated and only two crystals from one supplier were found acceptable. A capping technique, consisting of Si_3N_4 deposited by plasma deposition and a chemical vapor deposited SiO_2 film, was developed and used successfully on wafers implanted with a dose up to 10^{15}cm^{-2} and with anneal temperatures up to 900°C.

This process was tested using existing discrete device masks and two additional integrated circuit masks developed under a Company sponsored program. One of these mask sets was designed with a sample-and-hold circuit and a comparator and the other was a ripple counter mask with digital circuits with up to a 100 gate complexity. Results are detailed in Section 4.

In addition to the active layer implant process, boron isolation implant was demonstrated by fabricating planar TEDs. The isolation implant may not be needed for the all-FET circuits, but is likely to prove very useful in the FET-TED circuits if it proves necessary to start with vapor phase epi for the TED active channels.

1.4 CIRCUIT TECHNIQUES STUDY

The purpose of this task was to perform preliminary design studies of each of the building block circuits with a particular interest in further defining the device processing requirements and identifying any new design or processing constraints which might have emerged from the previous three tasks. A brief summary of the study conclusions follows:

- Amplifiers - Conventional design approaches with tuned interstage matching networks offer the best broadband performance. FET gate widths must be in excess of about 250 microns to reduce the input and output reflection coefficient magnitudes (S_{11} and S_{22}) to a value low enough to be impedance matched with on-chip reactive components. Inductors with values from one to 20 nanohenries will be

required. Monolithic amplifier noise figure performance will be somewhat degraded from MIC amplifier noise figure performance by the relatively low Qs of monolithic inductors.

- Oscillators - On-chip feedback type designs are very likely to be deficient in performance with regard to tuning range, temperature stability, and phase noise. These performance deficiencies are best relieved by incorporation of an off-chip tuning varactor. The oscillator will then consist of a single oscillating FET, off-chip varactor, monolithic bias circuitry, and a monolithic buffer amplifier. Preliminary studies indicate that a single VCO design can be made to operate over several different tuning ranges by appropriate varactor selection.

- Analog Multipliers - Since this circuit is the first building block test vehicle, its design was carried out in full detail. Four designs were initially proposed varying from a single dual-gate FET to a full transconductance multiplier. The two designs selected for implementation are described in detail in Section 5.3.

- Modulators and Demodulators - The modulator circuit was originally proposed for use as a spread spectrum despreader at the receiver front-end. Studies have shown that the TED/FET approach to this function is less likely to have good carrier suppression than the analog multiplier, and it will not be further pursued. In the other hand, the TED BPSK demodulator is so much simpler than the alternative (a Costas loop demodulator) that the choice between the two is very easy. We have had previous experience with this circuit, and chiefly need to incorporate the TED processing requirements into the overall process.

- Ancillary Circuit Functions - These circuit functions, which include filters, gain control functions and so forth were lumped with the previous circuits and considered as integral parts rather than separately.

1.5 PROCESS AND DEVICE DESIGN EVALUATION

The discrete FETs which were delivered are approximately equivalent in performance to NE244s, that is, they are good state-of-the-art 1 micron FETs. TEDs which operate at 5 GHz as logic AND and OR gates have been delivered. Section 6 describes the performance of the analog multiplier circuits which do in fact operate reasonably well to 10 GHz.

The six sections which follow are detailed descriptions of the Phase I tasks and appear in the same order as the preceeding dicussion. Additionally these are four appendices which give: an analytical description of the FET model (A), a listing of the FET model computer program (B), data from the process development work (C). and some analysis relating to the analog multiplier design (D). Appendix A is essentially a reprint of a report prepared for the Office of Naval Research under contract N00014-77-C-0645, and is included here for information purposes. The analysis described in Section 2 was all contract work except where otherwise stated.

2. MODEL DEVELOPMENT

2.1 GENERAL OPERATION OF THE FET MODELING CODE

A general block diagram of the FET code is shown in Figure 2-1. Upon entering the main control program, six options are available. Five of these are shown in the figure: ancillary region, dc analysis, variable parameter, detailed analysis, and doping optimization. The sixth is for rapid initialization of parameters and its use is followed by one of the other five options. The user may enter one option and have the calculations performed. Then a parameter can be changed and the option rerun or a new option chosen. After any calculation, output can be generated, such as a file for use with COMPACT, a computer aided design program, a tabulated file, or a file for plot generation.

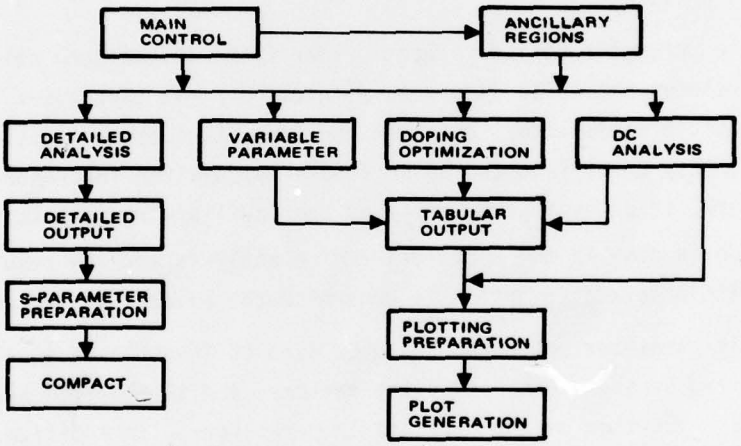


Figure 2-1. General Outline of FET Modeling Code

One mode of operation is to use the ancillary region option. This mode calculates the source-to-gate resistance R_s, the gate-to-drain resistance R_d, the gate metallization resistance R_g, the gate-to-drain capacitance C_{gd}, and the source-to-drain capacitance C_{sd}. The quantities are calculated from the physical character of the device, its dimensions, layout, and material properties. By exercising this option, one can optimize the region outside the active channel under the gate to reduce the value of the parasitics. Alternately, one can use the option to help determine material values from measured values of the parasitics. The analysis that occurs in each mode will be further considered in following sections.

Once the parasitics are calculated, the resulting values can be used in any of the four remaining options. The dc or noise figure analysis may be made using calculated parasitic values or values entered directly. In addition, analysis can be made for the intrinsic device alone without the effects of the ancillary regions.

The dc analysis calculates drain current vs drain and gate voltages. The resulting curves can be plotted or tabulated as a function of one of 11 parameters. Given a complete set of input parameters, the analysis is done immediately. If knowledge of a physical device is incomplete, this option can be used to match the measured dc curves to the predicted curves and thereby determine the unknown parameters. Because the dc analysis is used both for analysis and synthesis, it can be used in two ways. In the regular mode the dc analysis produces a detailed curve from the set of input parameters. When used for synthesis, a high speed mode is available which provides just six points for comparison to experimental results. The synthesis mode can also display noise figures as calculated from the TRW model and the Fukui equation for use as a reference when dc curves are fitted.

The variable parameter option is used primarily to investigate noise figures. This option calculates the noise figure as a function of 13 parameters. The parameters include the parasitic resistance. Although the parasitics are a function of many physical parameters, they enter into the noise figure calculation independent of their origin. Therefore, if a physical property of the ancillary regions is investigated, the investigation is done in the ancillary region analysis and the results are then used in the variable parameter option to determine the effects on the noise figure.

The variable parameter option can also be used to investigate scattering parameters. If desired S-parameters, stability factors, and the maximum available gain can be output as a function of the option's 13 parameters. In addition, the optimum source and load impedance and associated gain for minimum noise are calculated.

The variable parameter option can be used like the dc analysis to either analyze a set of input parameters or to synthesize a complete set given a limited number of input values and measurement results. Output from this option is in tabulated form with the option to plot the noise figure and gain as a function of the varied parameter.

For a given set of input parameters, one may choose the detailed analysis option. This option does not involve extended calculations, but provides a detailed output of calculated values. These values include external measurable quantities and internal quantities which are part of the model. The detailed analysis can be used to summarize the results for a particular device or to analyze the physical state of the device under given bias conditions.

The fifth option is listed in Figure 2-1 as a doping optimization routine. This option is the same as the variable parameter mode of operation with the exception that the doping density is varied at each point to search for a minimum noise figure. The option can be used to design devices when one has the freedom to choose the channel doping concentration.

A detailed breakdown of the FET code into subroutines is shown in Figure 2-2. The program is entered through MAIN from which one of six options can be chosen. Program operation is not automatic, but requires extensive user interaction, both to enter the initial configuration and to determine the course of action. Despite the amount of interaction required, the code is self-prompting and users with no previous experience can begin to use the code with very little coaching. To allow for both novice and regular users, the code includes short cuts which bypass the detailed prompting to reduce the running time once one is familiar with the code.

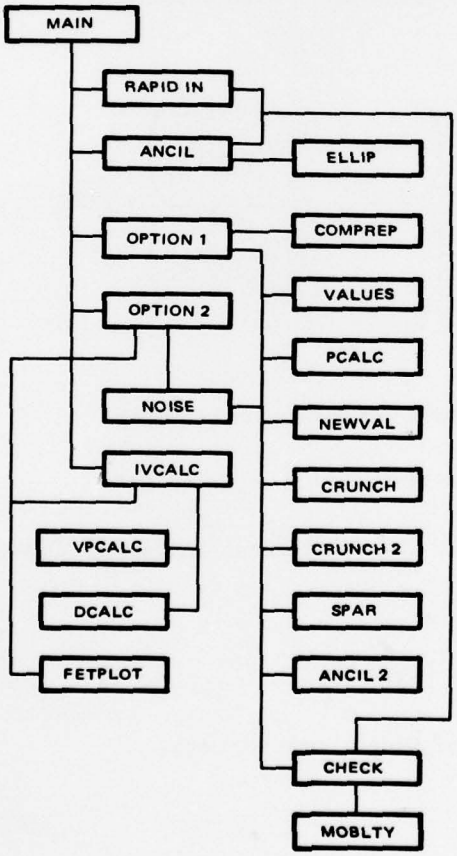


Figure 2-2. Diagram of the Modeling Code Subroutines and Their Basic Interconnections

The five subroutines accessed from MAIN in Figure 2-2 provide the available options in the program. After an option has been run, one can either revise parameters and rerun the option or return to MAIN to choose a new option according to the results of the previous run. The first option, RAPIDIN, is used to rapidly enter the input parameters for the initial device configuration. The parameters required are: gate length L, gate width Z, active channel depth a, operating temperature T, source-to-gate voltage V_{gg}, source-to-drain voltage V_{dd}, source series resistance R_S, drain series resistance R_d, gate metallization resistance R_g, operating frequency f, and channel doping concentration N_o. After the values are entered, they are checked and the user then chooses one of the remaining four options.

Although the parasitic resistances R_S, R_d, and R_g are initially input, their values can also be calculated. The second option listed in Figure 2-2 is ANCIL. This subroutine calculates the parasitic resistances and the source-to-drain and gate-to-drain capacitances, C_{sd} and C_{gd}, respectively. The analysis leading to the parasitic contribution is contained in Appendix A. From equation (6-9) of the appendix, the source resistance is given by

$$R_s = \frac{(\rho_{sco}\,\rho_c)^{1/2}}{Z} \frac{\left(1 + e^{-2\,\frac{(\rho_{sco})^{1/2}}{(\rho_c)^{1/2}}\,L_c}\right)}{\left(1 - e^{2\,\frac{(\rho_{sco})^{1/2}}{(\rho_c)^{1/2}}\,L_c}\right)} + \frac{\rho_{sch}\,L_1}{Z} + \frac{\rho_{shs}\,L_c}{2Z}$$

where

ρ_{sco} = sheet resistance of GaAs under contact metal

ρ_c = specific contact resistivity — metal to GaAs

ρ_{sch} = sheet resistance of channel between contact and gate

L_c = contact length

L_1 = contact to gate separation

ρ_{shs} = sheet resistance of source contact metal

Z = device width.

The first term represents the resistance of the contact metal and the metal-to-channel interface. the second term is the resistance of the channel between the contact and the gate. The third term is the resistance of the channel under the contact. The sheet resistance of the GaAs is calculated as

$$\rho_s = \frac{1}{q\mu_o n_o a}$$

q = electron charge

μ_o = mobility

n_o = doping concentration

a = channel depth

This form can be used either under a contact or between contacts by using the appropriate values of n_o and a for that region.

The gate resistance, R_g, depends on the geometry of the gate and its feed mechanism. ANCIL computes an early form for R_g as given by equation (6-10) of Appendix A

$$R_g \simeq \frac{\rho_{shg}\, Z}{2L}$$

where

ρ_{shg} = sheet resistance of gate metal

L = gate length

This form refers to an end-fed gate and does not include a skin effect term. Gates with different feed schemes, such as a single or double center-fed design, have lower resistances and as a result the skin effect term is more important. Alternate forms for the parasitics will be considered in the discussion of ANCIL2.

The source-to-drain and gate-to-drain capacitances are calculated by considering two metal strips inbedded at the boundary between two dissimilar dielectrics. From Section 6.4 of Appendix A, the capacitances are given by

$$C_{dg},\ C_{sd} = (\varepsilon_r + 1)\, \varepsilon_o Z\, \frac{K[(1 - k^2)^{1/2}]}{K(k)}$$

where K(k) is the complete elliptic integral of the first given by

$$K(k) = \int_0^{\pi/2} (1 - k \sin^2 \theta)^{-1/2} \, d\theta$$

The argument k depends on which capacitance is calculated. It is given by

$$k_{dg} = \left[\frac{L_{gd}}{L_{gd} + L} \right]^{1/2}$$

$$k_{sd} = \left[\frac{(2L_s + L_{sd}) L_{sd}}{(L_s + L_{sd})^2} \right]^{1/2}$$

In these equations

ε_r = relative dielectric constant of GaAs

ε_o = dielectric constant of free space

L_{gd} = gate-to-drain separation

L_s = source contact length

L_{sd} = source-to-drain separation

The complete elliptic integrals are computed numerically in function subroutine ELLIP.

The program flow in subroutine ANCIL is shown in Figure 2-3. When the subroutine is entered, it is first determined whether the input values must be set or updated. The input values consist of L_s, L_{sg}, L, L_{gd}, L_d, Z, a, n_o (under source), n_o (between source and gate), n_o (between gate and drain), n_o (under drain), ρ_L (source-to-channel), ρ_L (drain-to-channel), ρ_s (source metal), ρ_s (gate metal), and ρ_s (drain metal). In addition, two flags are set. One flag controls the form of the equations used to calculate R_s and R_d, depending on whether the contact resistance is to be included or not. The second flag determines the lateral doping profile to reduce the number of concentrations used when the device is symmetric.

To allow for faster operation of the progarm, all input parameters have default values. The total set of default values can be used to calculate the parasitics immediately, or some values can be changed first. Following the first call to ANCIL, one can use the current set of values or again make some changes first. As shown in Figure 2-3, after any changes are made, the values are checked to ensure that they do

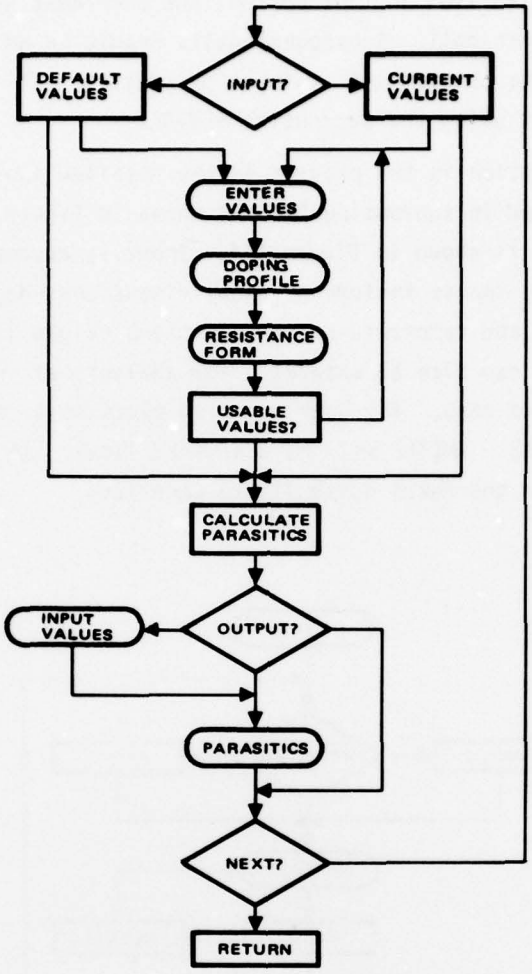


Figure 2-3. Program Flow in the Subroutine ANCIL. This subroutine calculates the parasitics for the ancillary region analysis.

not result in infinite operands during the calculation. If so, error messages are printed and control is returned to the parameter changing operation. This check is one of many included in the FET code to prevent fatal errors which will halt program execution. Such protection allows the program to be used by novice users.

After the parasitics are calculated, the operator may choose to have all the input parameters and the calculated parasitics printed, the parasitics only, or no listing at all. When ANCIL is used in the ancillary region analysis, one usually requires a full listing followed by a return to the input to change on input parameter. When ANCIL is used to provide values for another option, no listing is normally required because the parasitic resistances are always listed in the output heading.

When ANCIL is called from another option, the user must set up the input parameters only for the first call. Subsequent calls result in an automatic update of the parasitics using the current set of input parameters. It is possible, however, to revise the input set using the subroutine NEWVAL.

The third major option in the program is the detailed analysis of Figure 2-1. This option is performed in subroutine OPTION1 shown in Figure 2-2. Program flow through the subroutine is shown in Figure 2-4. Input is accomplished either through RAPIDIN or VALUES. The inputs include physical dimensions, doping density, bias conditions, frequency, and temperature. In addition, values for the parasitic resistances, R_s, R_g and R_d, can also be entered. For analysis of the intrinsic device, the parasitics can be set to zero. The user may also elect to have the resistances calculated by ANCIL or ANCIL2. ANCIL2 will be discussed later. It calculates resistances using the form found in the Fukui noise figure equation.

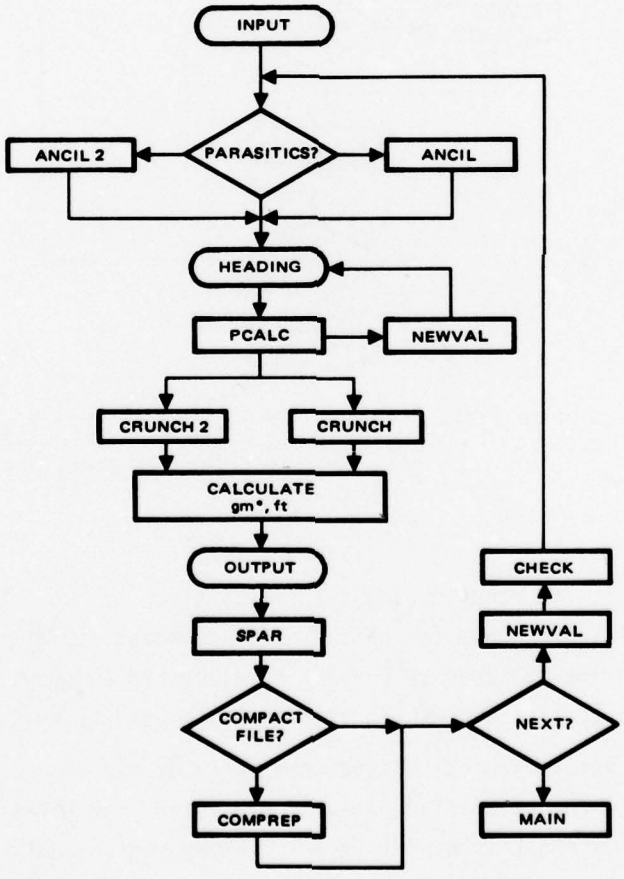


Figure 2-4. Program Flow in Subroutine OPTION1. This subroutine directs the detailed analysis.

Once the parasitics are determined, all input information is complete. From this information, the dc characteristics, the small signal parameters, and the noise figure can be calculated. The program flow of OPTION1 illustrates the point at which each of these sets of data is calculated. OPTION1 provides a summary of the calculated values.

Referring to Figure 2-4, once the input parameters are determined, OPTION1 prints a heading to identify the run and list the input parameters. Next, PCALC is called. This subroutine determines the dc operating point for the device with the given bias conditions. PCALC will be described following the discussion of the major options. PCALC finds the drain current, I_d, by solving for the normalized potential drop across the depletion region at the source end of the channel under the gate and at the boundary between the constant-mobility and velocity-saturated regions of the channel, s and p, respectively. In addition, the lengths of the regions L_1 and L_2 are determined. PCALC is only used if the device is properly biased in the current saturated region. If bias conditions have been chosen incorrectly, OPTION1 calls NEWVAL so they can be corrected and a new heading is printed.

The major calculations are done in the subroutine called CRUNCH or, when $L_1 = 0$, in CRUNCH2. These subroutines calculate the internal functions and the noise figure biased on the model described in Appendix A. The noise figure is found from the combination of the physical current fluctuations in the channel and the equivalent circuit for the device. Therefore, CRUNCH also calculates values for the equivalent circuit components. Two additional quantities are calculated - g_m^* and f_T. The terminal transconductance

$$g_m^* = g_m/(1 + g_m R_s)$$

is calculated from the intrinsic dc transconductance g_m and the cutoff frequency is given by

$$f_T = g_m/(2\pi C_{sg})$$

The cutoff frequency f_T is the frequency at which the gain becomes unity.

An example of the output from OPTION1 is shown in Figure 2-5. The heading identifies the run and is followed by a listing of the input parameters. Next, the noise figure and related values are given. The noise figure calculated from the empirical Fukui equation is also printed for reference. Next, the equivalent ciruit component values are listed. The Region I and Region II values refer to the constant mobility and saturated velocity regions, respectively. The additional parameters inlcude W_{oo}, the gate potential which will totally deplete the channel of carriers; g_o, a normallizing conductance; E_s, the electric field above which the electron

```
RUN 19   KU FET-2   1  SUMMARY

 GATE LENGTH      =   1.20 MICRONS          VGG =  -1.25 V
 GATE WIDTH       = 250.00 MICRONS          VDD =   3.00 V
 CHANNEL DEPTH    =    .22 MICRONS          RSG =  10.00 OHMS
 DOPING DENSITY   = 8.00E+16 ATOMS/CC       RGD =  20.00 OHMS
 DEVICE TEMP      = 300.00 K               RGATE =   4.00 OHM
 FREQ.            =  10.00 GHZ

          NF(FUKUI) = 3.633 DB
       NOISE FIGURE =  4.2361 DB
  TRANSCONDUCTANCE = 18.82   MMHO
       TERMINAL GM = 15.84   MMHO
 CUT-OFF FREQUENCY = 14.10   GHZ

 CAPACITANCE (PF)                      RESISTANCE (OHM)
                  INTRINSIC
 CSG = .2125                           RI (GATE CHARGE) =   11.29
 CGD = .0299                             RD (OUTPUT) = 4018.72
                  PARASITIC
 CSD = .0397                           RM (GATE METAL) =    4.00
                                         RF (SOURCE) =   10.00
                                         RDF (DRAIN) =   20.00

    REGION I                             REGION II
  L1 =  .525 MICRON                      L2 =  .675 MICRON
     = 43.72 %                              = 56.28 %
   S = .8517859                           P = .8798721

              ADDITIONAL PARAMETERS
  ID = -11.36 MA                          IS = -94.58 MA
 W00 = -2.802 V                          PHI =  -.670 V
  G0 = -1.305 MMHO                    SATDEX =  -.124
  ES =  2.900 KV/CM                      MU0 = 4627.0 CM2/V/SEC
  VS = 1.34E+07 CM/SEC                DIFCON =  100.0 CM2/SEC
                                       DIELC =  1.107 PF/CM

 S11:    .745    < -70.9     S12:    .128    <  42.8
 S21:   1.074    < 112.9     S22:    .887    < -28.3
 OPTIMUM SOURCE   .794  <  38.3     OPTIMUM LOAD   .706  <  30.9
 K=  .586   DEVICE NOT INHERENTLY STABLE


 CREATE FILE FOR COMPACT? (1=YES)
? 0
 NEXT, MAKE A REVISED RUN (-1), CHANGE OPTION (0) OR
 CONCLUDE SESSION (1)?
? 1
```

Figure 2-5. Example of Printout Produced by the Detailed Analysis of OPTION1

velocity is saturated; v_s, the saturated velocity; I_s, a normalizing current; ϕ, the built-in potential which arises across the Schottky barrier; ξ, the saturation index; μ_o, the mobility; D, the high field diffusion constant; and $\varepsilon_r\varepsilon_o$; the absolute dielectric constant of GaAs.

The remainder of the printout in Figure 2-5 lists the S-parameters (magnitude and angle) followed by the optimum source and load impedance required for minimum noise and the stability factor for the device. These quantities are calculated from the equivalent circuit component values in the subroutine SPAR and represent the small signal parameters. For circuit design, both the small signal parameters and the equivalent circuit component values are used.

Once output has been completed, the equivalent circuit values can be combined in a file that can be submitted to COMPACT. COMPACT is a commercial circuit design program which in addition to analyzing a circuit to find S-parameters, gain, and other small signal parameters, can be used to optimize the values of additional components such as matching elements to meet the desired circuit design goals. The COMPACT file is created in subroutine COMPREP.

At the completion of a run through OPTION1, the user can return to MAIN for a different option or change an input parameter in NEWVAL and rerun the option. Subroutine CHECK which follows NEWVAL in the flow chart of Figure 2-4 determines if the parameter change has resulted in the channel being pinched off. CHECK calculates the mobility, μ_o, using the function MOBILITY and the built-in potential, ϕ.

To investigate the model predictions or to design devices, OPTION2 is used. Two modes of operation, the variable parameter mode and the doping optimization mode of Figure 2-1, use OPTION2. The subroutine is basically similar to OPTION1 in the way calculated values are obtained. However, OPTION2 is complicated by a code which varies one of the input parameters through a range of values. At each value of the parameter, several values are output. The outputs included: the variable x, I_d, g_m*, g_m, NF, f_T, W_{oo}, and G (the associated gain). In addition, the noise figure as calculated from the Fukui equation is included for reference.

The program flow is diagramed in Figure 2-6. Input involves the use of either RAPIDIN or VALUES. As in OPTION1 the parasitics may be calculated in ANCIL, calculated in ANCIL2, input directly, or set to zero for an intrinsic region analysis. Next, the parameter to be varied must be chosen and the range and step size input. The allowable variables are: L, Z, a, N, T, V_{gg}, V_{dd}, R_s, R_d, f, ϕ, R_g, and D. At this point in the program it is possibly to designate that the gate bias be set to a fraction of pinchoff rather than to a fixed value. Following the input procedure, the heading is printed out.

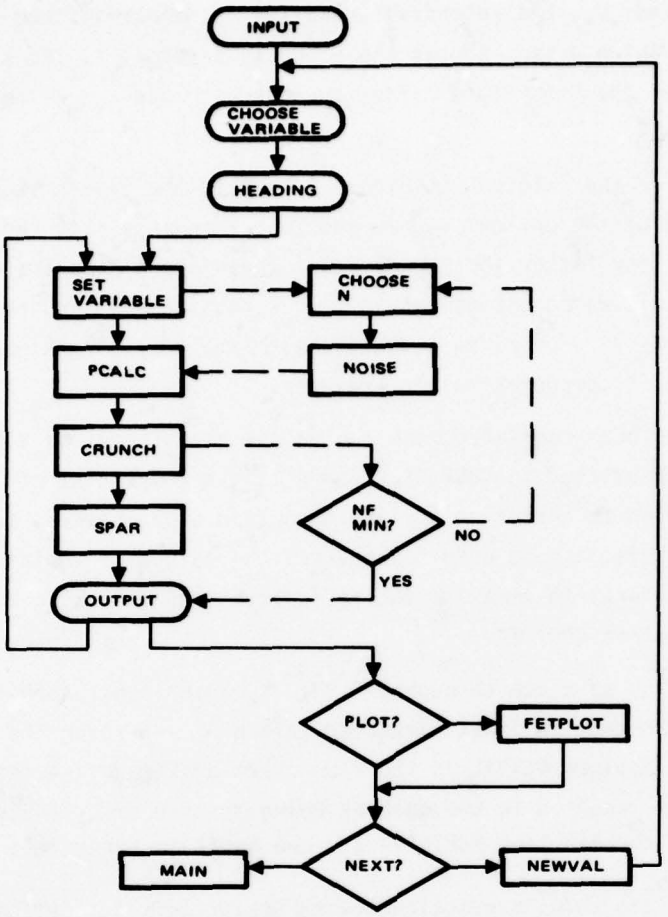


Figure 2-6. Program Flow in OPTION2. This subroutine performs the variable parameter analysis. Functions appended with dashed lines are used for the doping optimization mode.

OPTION2 then begins to step through the range of values for x, the variable parameter. When a value of x is calculated, the parasitics are updated in ANCIL (or ANCIL2) if necessary and CHECK is called. Next, PCALC, CRUNCH (or CRUNCH2), and SPAR are called as in OPTION1. An example of the tabulated output is shown in Figure 2-7. For the example shown, the gate bias has been varied to provide a listing of output parameters. If the option to include S-parameters is desired, the S-parameters and stability factor are also printed for each value of the varied parameter.

After the table (Figure 2-7) is printed, the data can also be plotted. If FETPLOT is called, the noise figure and associated gain are plotted as a function of the variable parameter, x. Next, OPTION2 can be rerun with any input parameters changed in NEWVAL. One may also branch back to MAIN to choose a different option or conclude the session.

```
RUN 16  NOW AT 10 GHZ  D = 100

 GATE LENGTH      =   1.20 MICRONS          VGG =  -2.00 V
 GATE WIDTH       = 250.00 MICRONS          VDD =   3.00 V
 CHANNEL DEPTH    =     .22 MICRONS         RSG =  10.00 OHMS
 DOPING DENSITY   = 8.00E+16 ATOMS/CC       RGD =  20.00 OHMS
 DEVICE TEMP      = 300.00 K              RGATE =   4.00 OHM
 FREQ.            =  10.00 GHZ
```

VGG	ID	GMT/GM	N.F.	FT	W00	GAIN
	NF(FUKUI) = 3.633 DB					
0.00	-33.7	20.72/26.13	8.0975	14.80	-2.80	10.23
	NF(FUKUI) = 3.633 DB					
-.25	-28.7	19.44/24.14	7.3431	14.66	-2.80	10.00
	NF(FUKUI) = 3.633 DB					
-.50	-24.0	18.37/22.50	6.6016	14.52	-2.80	9.79
	NF(FUKUI) = 3.633 DB					
-.75	-19.6	17.44/21.12	5.8507	14.37	-2.80	9.59
	NF(FUKUI) = 3.633 DB					
-1.00	-15.4	16.61/19.92	5.0696	14.24	-2.80	9.41
	NF(FUKUI) = 3.633 DB					
-1.25	-11.4	15.84/18.82	4.2361	14.10	-2.80	9.22
	NF(FUKUI) = 3.633 DB					
-1.50	-7.5	15.05/17.71	3.3276	13.95	-2.80	9.02
	NF(FUKUI) = 3.633 DB					
-1.75	-3.9	13.92/16.17	2.3500	13.73	-2.80	8.72
	NF(FUKUI) = 3.633 DB					
-2.00	-.8	9.96/11.06	1.6808	12.61	-2.80	7.38

```
 DO YOU WANT A NOISE FIGURE PLOT?(1=YES)
? 0

NEXT, MAKE A REVISED RUN (-1), CHANGE OPTION (0)
OR CONCLUDE SESSION (1)?
```

Figure 2-7. Example of Program Output Using OPTION2. Output is generated as a function of gate voltage.

Subroutine OPTION2 is also used for the doping optimization mode of operation. When the optimization option is chosen, the program flow shown in Figure 2-6 includes the flow shown with dashed lines. After the variable x is set, a doping concentration is chosen (first value is $1 \times 10^{17}/cm^3$). With this value, subroutine NOISE then calls ANCIL, PCALC and CRUNCH to determine the noise figure. If the noise figure is not at a minimum, the doping concentration is changed and a new noise figure is calculated The option searches over a range of $1 \times 10^{16} < N < 1 \times 10^{18}$ and requires that it be possible to calculate a noise figure at $N = 1 \times 10^{17}$, the first point.

That last major option listed in the FET code subroutine list of Figure 2-2 is IVCALC which does the dc analysis. The dc analysis involves generating values of drain current for a given value of gate voltage by varying the drain voltage. Figure 2-8 shows the program flow in the subroutine. Upon choosing option IVCHAR, one can choose either the regular mode of operation or a high speed mode. In the regular mode, 30 pairs (V_{dd} and I_d (V_{dd})) are calculated. In the high speed mode, only six pairs are calculated. Next, the input parameters are inlcuded using either VALUES or RAPIDIN.

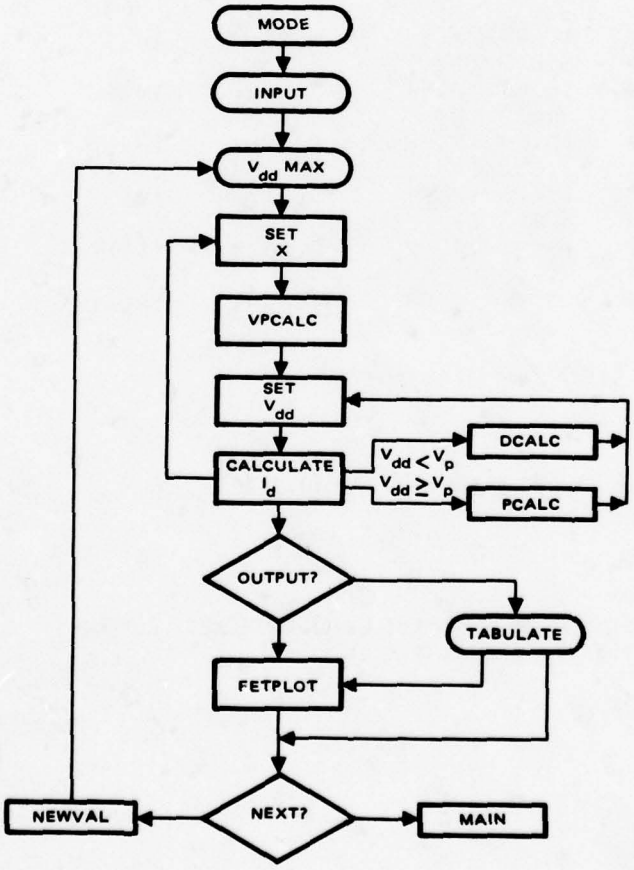


Figure 2-8. Program Flow in Subroutine IVCHAR. This subroutine does the dc analysis.

Finally, three additional inputs are made. The first is the maximum value of drain voltage that one is interested in. The final range of V_{dd} will be from 0 to this maximum value. Second, the form of the drain resistance can be input. IVCHAR uses the form

$$R_d = A + B|V_{gg}|$$

where A and B are input by the user. Parameter A is related to the channel resistance plus DRAIN contact resistance plus drain metal resistance as shown in Appendix A. The second term describes the increase in drain resistance due to the extension of the depletion region toward the drain contact. The parameter B must be chosen empirically. In fact, some depletion may be present outside the gate region even at $V_{gg} = 0$, because of the presence of the built-in potential. Therefore, A can also be larger than the calculated value and can be determiend empirically from the $V_{gg} = 0$ I-V curve. The third input is the parameter to be varied, its range, and the step size. Usually, one desires I-V curves as a function of V_{gg}. However, it is also convenient to generate curves as a function of R_d to determine the empirical parameters A and B. IVCHAR allows one to generate curves as a function of L, Z, a, N, T, V_{gg}, R_s, R_d, and Ø.

As shown in Figure 2-8, after the input functions are complete, IVCHAR sets the first value of the variable parameter x. If necessary, ANCIL is called to update the parasitic resistances. Then the program calls VPCALC. VPCALC computes the drain voltage, V_p, at which carriers just reach their saturated velocity at some point in the channel. This point corresponds to the begining of current saturation for the device. After V_p is determined, IVCHAR loops through either 6 or 30 values of V_{dd}, depending on the operating mode chosen. For a given drain voltage, the drain current is calculated by DCALC if $V_{sd} < V_p$ or PCALC if $V_{sd} \geq V_p$. Voltage V_{sd} is the source-to-drain voltage across the intrinsic device.

Although not shown in Figure 2-8, when using the high speed mode, the six pairs of values are printed as soon as they are calculated. The program then pauses to allow the user to decide whether to proceed to the next value of x or drop immediately to the end of the subroutine and ask for the next course of action. Thus the high speed mode allows the user to run through IVCHAR several times, adjusting parameters until values are obtained which give good agreement between predicted and empirical I-V curves. The regular mode of opeation computes all the data before the output mode is determiend. The output is either in tables, as a plot, or both. The plots are generated using FETPLOT. Finally, the user can rerun the option after changing parameters in NEWVAL or return to MAIN to choose a new option or conclude the session.

An example of the output of IVCHAR using the high speed option is shown in Figure 2-9. In the figure, the gate voltate is being changed in steps of 0.25 V if the user chooses to continue. Above each set of (V_{dd}, I_d) values, the parasitic resistances (R_s, R_d, R_g) are printed along with the value of the varied parameter (V_{gg} for this example) and the drain voltage at which the current saturates. Below the I-V data, some noise figure data is also included for reference.

Returning to the subroutine listing of Figure 2-2, each of the mjaor subroutines (ANCIL, OPTION1, OPTION2, and IVCHAR) has been discussed. Except for ANCIL, these routines manage the options but do not make the calculations. ANCIL and ANCIL2 calculate the parasitics. VPCALC, PCALC, and DCALC are used to compute the drain current for a given set of bias conditions and physical device parameters. Therefore, these three subroutines determine the dc characteristics. CRUNCH and CRUNCH2 calculate the funtions that lead to the noise figure and equivalent circuit. The noise figure calculation depends on the division of the channel into unsaturated and velocity saturated regions, as computed in PCALC. Finally, SPAR uses the equivalent circuit values and optimum source and load impedance as calculated in CRUNCH to evaluate the S-parameters, maximum gain, and associated gain for the device.

Subroutine PCALC determines the drain current from the basic assumption of the Pucel model, that the channel may be divided into two regions as described in Appendix A, Section 2. The channel, so divided, is described by two reduced potentials, s and p, which are related to the voltage drop across the depletion region. Potential s is the drop across the depletion region at the leading or source end of the gate. Potential p is the drop at the boundary between Region I and Region II. To find s and p, two equations are solved simultaneously

$$s^2 = \frac{V_{gg} + I_s (1 - p) R_s + \phi}{W_{oo}}$$

and

$$0 = V_{dd} + I_s (1 - p) (R_s + R_d) + W_{oo} \left(p^2 - s^2 - \xi \sinh \left[\frac{(L - L_1)}{2a} \right] \right)$$

where

$$L_1 = \frac{-W_{oo} f_1}{E_s (1 - p)}$$

$$f_1 = p^2 - s^2 - \frac{2}{3} (p^3 - s^3)$$

```
RUN 9   IV CURVES AGAIN

 GATE LENGTH      =   1.20 MICRONS          VGG =   0.00 V
 GATE WIDTH       = 250.00 MICRONS          VDD =   3.00 V
 CHANNEL DEPTH    =    .22 MICRONS          RSG =  10.00 OHMS
 DOPING DENSITY   = 8.00E+16 ATOMS/CC       RGD =  20.00 OHMS
 DEVICE TEMP      = 300.00 K              RGATE =   2.00 OHM
 FREQ.            =  10.00 GHZ


 RSG =  10.0      RGD =  20.0      RGATE =  2.0
 VGG =  0.00 V.   VPINCH = VSD AT VDD =  1.225 V
         VDD (V)       DRAIN CURRENT (MA X -1)

             .500          13.071
            1.000          25.348
            1.500          32.400
            2.000          33.092
            2.500          33.442
            3.000          33.681
             NF(FUKUI) = 3.446 DB
                           20.72/26.13     5.1060     14.80      -2.80   10.23
 CONTINUE?  (1=YES)
? 1
 RSG =  10.0      RGD =  22.5      RGATE =  2.0
 VGG =  -.25 V.   VPINCH = VSD AT VDD =  1.143 V
         VDD (V)       DRAIN CURRENT (MA X -1)

             .500          11.823
            1.000          22.804
            1.500          27.631
            2.000          28.183
            2.500          28.486
            3.000          28.697
             NF(FUKUI) = 3.446 DB
                           19.44/24.13     4.5705     14.66      -2.80   9.99
 CONTINUE?  (1=YES)
? 1
 RSG =  10.0      RGD =  25.0      RGATE =  2.0
 VGG =  -.50 V.   VPINCH = VSD AT VDD =  1.046 V
         VDD (V)       DRAIN CURRENT (MA X -1)

             .500          10.631
            1.000          20.430
            1.500          23.121
            2.000          23.562
            2.500          23.822
            3.000          24.009
             NF(FUKUI) = 3.446 DB
                           18.36/22.48     4.0547     14.51      -2.80   9.78
 CONTINUE?  (1=YES)
```

Figure 2-9. Example of the Output Produced by IVCHAR. Current-voltage pairs are generated as a function of gate voltage.

These equations are similar to those derived in Section 2 of Appendix A, but include the voltage drops that occur across R_s and R_d. After input parameters have been assigned values, these equation contain only two unknowns, s and p. To find s and p, an initial choice for s is used

$$s_{int} = \frac{V_{gg} + \phi}{W_{oo}}$$

and p is solved-for knowing that p lies in the range $s < p < 1$. Using the value of p determined from s_{int}, a new value of s is found and the process of finding p is repeated. In practice, s and p are found to four-place accuracy in about three or four iterations.

The drain current has then been found since

$$I_d = I_s (1 - p)$$

To calculate V_p, subroutine VPCALC uses the same equation for s^2. However, the second equation is taken from the expression for L_1. When current saturation first occurs, the voltage across the intrinsic device

$$V_{sd} = V_{dd} + I_d (R_s + R_d)$$

$$= V_p$$

and for $V_{sd} \leq V_p$, $L_1 = L$. Therefore, the equation for L_1 becomes

$$L = \frac{-W_{oo} f_1}{E_s (1 - p)}$$

or

$$0 = \xi (1 - p) + f_1$$

When these equations are solved for s and p, V_p can be found from the second equation used in PCALC using $L - L_1 = 0$

$$V_p = -W_{oo} (p^2 - s^2)$$

The third of the dc current calculating subroutines is DCALC. This routine is used to calculate I_d when $V_{sd} < V_p$ or when the device is biased below saturation. For this bias condition, the reduced potential across the depletion region at the drain end of the gate is denoted by d. Then s and d are given in terms of I_d as

$$s^2 = (V_{gg} + I_d R_s + \phi)/W_{oo}$$

$$d^2 = (V_{gg} - I_d R_d + \phi - V_{dd})/W_{oo}$$

A third equation in I_d is taken from Eq. (2-19) in Appendix A

$$I_d = \frac{- g_o Z W_{oo}}{L_1} f_1$$

Below saturation, $L_1 = L$ and this equation can be used with p = d. Therefore, DCALC solves

$$0 = I_d + \frac{g_o Z W_{oo} f_1}{L}$$

where $f_1 = d^2 - s^2 - \frac{2}{3}(d^3 - s^3)$ in combination with the expressions above to find the current I_d.

The majority of the calculations done by the FET modeling code are accomplished in CRUNCH or CRUNCH2. Although many functions are evaluated in CRUNCH, all the solutions are anlytical and no iterative schemes need be used to obtain values. The subroutine calculates the following output parameters: r_d the output resistance, C_{sg}, g_m, f_T, R_i the gate charging resistance, NF, $Z_{s,opt}$ the optimum source impedance for low noise operation, and NF (Fukui) – the noise figure derived from the Fukui empirical equation. To obtain these results, CRUNCH evaluates all of the internal functions of p and s that are derived in Appendix A. These functions include: f_1, f_2, f_3, f_g, f_r, f_c, Y, k, k', K' ($\gamma = 0$), R_o, R_δ, S_o, S_δ, P_o, P_δ, P_1, P_2, R_1, R_2 and the NF functions C, K_g, K_c, and K_r.

The optimum source impedance $Z_{s,opt}$ is given by

$$Z_{s,opt} = R_{s,opt} + i X_{s,opt}$$

in which the components are described in Section 4 of Appendix A. The Fukui noise figure is calculated from

$$NF\ (Fukui) = 10 \log\ 1 + 0.033\ f\ L^{5/6}\ \frac{N}{a}^{1/6}\ Z^{1/2}\ (R_s + R_g)^{1/2}$$

in which the factor 0.033 is an empirically determined value and the remainder of the variables are entered in the appropriate units.

The forms of the parasitics as normally used in the Fukui equation are contained in ANCIL2. CRUNCH computes both noise figures using the same values of R_s and R_g. Therefore, the second form for the parasitics contained in ANCIL2 may be used as an alternate to the forms in ANCIL. In ANCIL2, the source-to-gate resistance has two terms

$$R_s = \frac{1.8\ L_{sg}}{N\ a\ Z} + \left(\frac{0.18\ R_c}{N\ a\ Z^2}\right)^{1/2}$$

where R_c is the specific contact resistance. The first term is the bulk resistance in the source-to-gate region of the channel. The second term gives the contact resistance. The gate resistance is given by

$$R_g = \frac{3.3\ \rho\ Z}{h\ L\ K_{feed}} + 0.6\ Z\ \left(\frac{\rho\ f}{hL}\right)^{1/2}$$

where

ρ = gate metallization resistivity

h = gate metal thickness

K_{feed} = constant dependent on the gate geometry

The first term is the resistance of the gate metal. If the gate is end-fed, $K_{feed} = 1$. For a center fed gate, $K_{feed} = 4$. The second term in the R_g expression is the resistance due to the skin effect as indicated by the frequency dependence.

The last subroutine of special interest is CRUNCH2. This subroutine represents an extension of the original Pucel derivation. The basic assumption is that the gate region can be divided into two parts. However, for very short gates, the analysis leads to a breakdown in the equations because Region II extends across the entire intrinsic region. To overcome this limitation, the equations have been rederived for a completely saturated gate region. These equations are contained in CRUNCH2. If this condition

occurs, it is detected in PCALC and the following action is taken: $p = s$, $L_2 = L$ and a flag is set to call CRUNCH2 when calculating the noise figure.

From the derivation for $L_1 \to 0$, the noise figure is given by

$$NF = 10 \log \left[1 + 2 \frac{f}{f_T} \left[K_g g_m \frac{T}{300} (R_s + R_g) \right]^{1/2} + 2 \left(\frac{f}{f_T} \right)^2 K_g g_m \left[\frac{T}{300} (R_s + R_g) + K_c R_i \right] \right] + \ldots$$

where R_i is the gate charging resistance. The noise coefficients K_g and K_c are given by

$$K_g = P_2 \left(1 - \frac{L}{apf_c} \right)^2$$

$$K_c = \frac{1}{\left(1 - \frac{L}{apf_c} \right)}$$

where

$$f_c = \frac{L}{ap} + 1.56$$

The noise generated in the channel by dipole drift is described by P_2 which has the form.

$$P_2 = \frac{L (1 - p) f_3}{a\xi f_r^2 f_g}$$

where

$$f_3 = \pi^3 \frac{16D}{D_o} \left(\frac{\sin \frac{\pi}{2}(1-p)}{\frac{\pi}{2}(1-p)} \right)^2 \left(\exp \left(\frac{\pi L}{a} \right) - 4 \exp \left(\frac{\pi L}{2a} \right) + \frac{\pi L}{a} + 3 \right)$$

$$f_r = 2p \left(\cosh \left(\frac{\pi L}{2a} \right) - 1 \right)$$

$$f_g = \frac{1}{2p}$$

The coefficients D_o and D are the low and high field diffusion constants, respectively, for electrons in GaAs.

The resulting equations are less complex than the corresponding equations in Section 4 of Appendix A. The simplification occurs for two reasons. First, no contribution is included for region I generated noise because no region I is assumed to exist. Second, dipole drift noise generated in region II is fully correlated with the noise coupled to the gate. Therefore, the correlation coefficient is 1.

2.2 SPECIFIC FORM OF THE FET MODELING CODE

A listing of the FET modeling code is included as Appendix B. The common blocks listed at the beginning of program MAIN (p. B-1) contain the input and output parameters which are transferred between subroutines. The first common block contains constants. The variable names are identified in Table 2-1. The mobility is only a constant for a given doping concentration and temperature. Its value is determined in MOBLTY, p. B-51 of the code. The high field diffusion constant, D, has also lost its status as a constant. Comparison of model predictions to experimental values indicate that the originally proposed value of 35 cm^2/sec may be too low, particularly for short gate FETs in which lateral electric fields become much higher. As noted in the discussion of OPTION2, the present code can vary D if desired.

The second common block contains the external parameters or physical parameters of the device. The variables are identified in Table 2-2. The variables GL to F in common block EXTPAR correspond to quantities already discussed. The remaining variables are to be used for a variable vertical doping profile. The first, IPROFIL is used to specify the form of the doping profile. DOPIN is an array which is filled with values of doping concentration as a function of depth. This array can be used when a nonanalytic profile is used. The second array, DOP is the value of N at 100 levels throughout the channel. DOP is determined either from the analytic form or by interpolating over the range of values contained in DOPIN. The last two arrays DOPB and DOP2B correspond to $\overline{N(y)}$ and $\overline{\overline{N(y)}}$, respectively. These arrays evaluate the functions

$$\overline{N(y)} = \int_0^y N(y)\, dy$$

$$\overline{\overline{N(y)}} = \int_0^y \overline{N(y)}\, dy$$

which are used for the variable vertical doping profile as described in Appendix A, Section 5.

The variable vertical doping profile analysis is presently done in a separate subprogram. The program was developed separately to facilitate testing of the equations and the evaluation procedure. Now that the form of the equations has been verified, the appropriate computer code is being incorporated in the master program listed in Appendix B. The inclusion of the integral arrays, DOPB and DOP2B, represent the beginning of the incorporation process.

The third common block, CALC, contains the first set of calculated parameters. Table 2-3 lists and identifies the variables in CALC. These parameters are determined in either subroutine CHECK or PCALC and constitute the dc parameters. The small signal parameters are contained in common block PAROUT. The variables are listed in Table 2-4. These variables are determined in CRUNCH. They consist of the noise figure and the equivalent circuit component values. The optimum source impedance, RSOPT + i XSOPT, is transferred to SPAR where it is used to calculate the gain associated with minimum noise operation.

Common block TOPLT contains the arrays which are to be plotted. Table 2-5 defines the variables. The X-axis may be any of the variable parameters of OPTION2. When OPTION2 is used the array FY contains the calculated noise figures and array FG contains the associated gain. These arrays are transferred to subroutine FETPLOT in which the values are ordered and written onto a file. The file is automatically processed by a plotting program which calls the appropriate plotting routines to generate the graph. When called from OPTION2, FETPLOT produces graphs with two curves on them, noise figure and associated gain. When called from IVCHAR, FETPLOT produces from 1 to 10 curves of I_d vs V_{dd} as a function of V_{gg} or some other variable.

The final common block, ANCPAR, contains the physical parameters required for the parasitic element calculations. The variables are identified in Table 2-6. These variables are only used in subroutine ANCIL and are not transferred to another subroutine. They are included in a common block to prevent their memory locations from being written over as the program shifts between subroutines.

Table 2-1. Variable Names Stored in Common Block CONSTS

ECHARGE	Electron charge, -1.6×10^{-19} Coul
AMUO	Mobility (cm^2/V sec)
ESAT	Saturation electric field, 2.9 KV
DIELC	Absolute dielectric constant of GaAs, 1.1 pf/cm
BOLTZK	Boltzmann's constant, 1.4×10^{-23} erg/^oC
DIFCON	High field diffusion constant (cm^2/sec)
PI	3.14

Table 2-2. Variable Names Stored in Common Block EXTPAR

GL	Gate length (cm)
Z	Gate width (cm)
A	Active channel depth (cm)
DOPEC	Channel doping concentration (atoms/cm^3)
T	Temperature (K)
VGG	Voltage applied to gate with respect to the source (V)
VDD	Voltage applied to drain with respect to the source (V)
RPF	Source-to-gate resistance (Ω)
RPDR	Gate-to-drain resistance (Ω)
RPM	Gate metallization resistance (Ω)
ATITLE	A 70 character array which holds a descriptive title
PHI	Built-in potential (V)
F	Frequency (Hz)
IPROFIL	Type of vertical doping profile
DOPIN	Input doping profile array (10^{16} atoms/cm^3)
DOP	Interpolated doping profile array (atoms/cm^3)
DOPB	Integral of doping profile (atoms/cm^2)
DOP2B	Double integral of doping profile (atoms/cm)

Table 2-3. Variable Names Stored in Common Block CALC

P	Normalized depletion depth at the Region I - Region II interface
S	Normalized depletion depth at the source end of the gate
GO	Sheet conductivity of the channel (Ω^{-1})
AISAT	Normalizing or saturation current (A)
AID	Drain current (A)
WOO	Gate potential which totally depletes the channel (V)
SATDEX	Saturation index, a parameter which describes the importance of velocity saturation
ARGU	$\pi L/2a$, used as the argument of several functions

Table 2-4. Variable Names Stored in Common Block PAROUT

FMIN	Minimum noise figure (dB)
GM	Transconductance (mho)
CSG	Source-to-gate capacitance (F)
CGD	Gate-to-drain capacitance (F)
CSD	Source-to-drain capacitance (F)
RPI	Gate metallization resistance (Ω)
GL1	Length of Region I (cm)
GL2	Length of Region II (cm)
RD	Output resistance (Ω)
RSOPT	Real part of optimum source impedance for minimum noise
XSOPT	Imaginary part of optimum source impedance for minimum noise

Table 2-5. Variable Names Stored in Common Block TOPLT

FX	X-axis values
FY	Y-axis values
FG	The gain associated with noise figures of array FY
NPT	Number of data points in a curve
NLN	Number of lines to be plotted

Table 2-6. Variable Names Stored in Common Block ANCPAR

SSG	Source to gate separation (cm)
SL	Source contact length (cm)
DOPES	Doping concentration under source (atoms/cm^3)
DOPESG	Doping concentration between source and gate (atoms/cm^3)
RSCS	Specific contact resistance of source (Ω - cm^2)
RSHS	Sheet resistance of source contact metal (Ω/)
RSHG	Sheet resistance of gate metal ($\Omega/\square$)
SGD	Gate to drain separation (cm)
DL	Drain contact length (cm)
DOPED	Doping concentration under drain (atoms/cm^3)
DOPEGD	Doping concentration between gate and drain (atoms/cm^3)
RSCD	Specific contact resistance of drain (Ω - cm^2)
RSHD	Sheet resistance of drain contact ($\Omega/\square$)
IREG	Form to be used to calculate R_s and R_d
ISYM	Amount of symmetry in the lateral doping profile

2.3 SUBPROGRAM TO EVALUATE VARIABLE VERTICAL DOPING PROFILE

A subprogram has been written in BASIC which performs the calculations indicated in Appendix A. Section 5 of Appendix A deals with the variable doping problem and presents results which can be compared with Pucel's paper or the other sections of the Appendix.

A complete listing of the subprogram is included in Appendix B. The first portion of the program includes the variable doping density profile and calculates certain functions of N(w) required later. These are

$$A(w) = \int_0^w N(w)\, dw = \overline{N(w)}$$

where w is depth normalized by active layer thickness.

$$B(w) = \int_0^w w\, N(w)\, dw$$

$$C(w) = \int_0^w w\, N(w)\, \overline{N(w)}\, dw = \int_0^w w\, N(w)\, A(w)\, dw$$

Other similar functions are calculated later as needed. The program calculates A(w), B(w), C(w) step by step, and stores each value A(I), B(I), C(I) in arrays.

The determination of the quantities s and p representing the fractional depletion depths at the source and gate ends of the device is obtained by simultaneously solving two relationships containing these quantitites — just as in Pucel's paper. The problem is solved by writing these relationships in terms of two subscripts I and J, where changes in s correspond to steps in I and changes in p to steps in J.

The functions of s and p such as the function $f_1(s,p)$ in Appendix A (Equation (Equation 5-19)

$$f_1(s,p) = \overline{N(1)} \int_0^p w\, N(w)\, dw - \int_0^p w\, N(w)\, \overline{N(w)}\, dw$$

can thus be written

$$F(I,J) = A(N_1)\left[B(J) - B(I)\right] - \left[C(J) - C(I)\right]$$

by remembering that the integrals are represented by the quantities B(I), C(I), etc.

The solution of the two simultaneous equations is thus changed from the solution of equations of the form:

$$f(s,p) = 0$$

$$g(s,p) = 0$$

to the solution of two equations of the form

$$F(I,J) = 0$$

$$G(I,J) = 0$$

A solution is found when I and J satisfying or nearly satisfy the equations. This is accomplished by stepping the quantities until the solution is bracketed and getting the final estimate by interpolation.

The following is an examination of the subprogram line by line.

Lines 100-220 Introduces program, calculates certain constants and dimensions arrays.

300-333 Puts in doping profile

335-363 Calculates the A(I), B(I), C(I) using a step-by-step integration

390-430 Prints pinch-off voltage; accepts V_{gg} (gate bias) also puts in drain resistance and built in potential

440-700 Solves two simultaneous equations to get s and p for the situation where L_2 is zero. Thus the saturation field is not reached until the drain end of the device.

The two functions FNS(I,J) and FNY(I,J) represent the relationships:

$$-V_{gg} + I_d R_1 - V_{sg} = 0$$

and

$$L_2/L = 0 \text{ or } 1 - L_1/L = 0$$

The functions are written in the form shown using (5-21) for I_d, (5-26) for L_1 and (5-11) to represent V_{sg}. The equation numbers are from Appendix A.

710-780 Calculates A1, A2, etc., which represent A(s) and A(p), the values of the function A for the determined values of S, p

Also calculated are B1, B2, etc.

The value of V_{DD}, the drain voltage just producing saturation, is printed out.

790-820 Accepts an input value of V_{dd}. If V_{dd} is larger than just calculated a saturation solution is carried out. If V_{dd} is less than calculated, program branches to end for subsaturation calculation.

830-980 Saturation solution; solves two simultaneous equations when $L_2 \neq 0$ in manner similar to earlier calculation. The function FNW(I,J) represents V_{sd} (see 5-25). The function FNV(I,J) represents the quantity

$$V_{dd} - V_{sd} - I_d (R_1 + R_2)$$

Solve FNV(I,J) = 0 and FNS(I,J) = 0 (again) simultaneously.

990-1040 Calculates the A(s), A(p), B(s), B(p), C(s), C(p) for this bias condition

1042-1048 Calculates another integral appearing

$$\int_s^p w\, N(w) \left[A(w)\right]^2 dw$$

1070-1140 Calculates L_1, L_2 (actually L_1/L, L_2/L), the g_m(G$), r_d (R$) and prints out s, p, I_D, g_m, r_d and g_m+. (5-27 through 5-30)

1150-1200 Calculates source gate capacitance (5-32 through 5-34) and the gate charging resistance and transit time. (See 5-35 to 5-37.) (A factor of 4 is included in calculating R_i to give a better fit.)

1210-2030 Are calculations of the various noise quantities discussed in Section 5.2 of the Appendix A. The program represents a direct evaluation of these quantities (P_o, P_d, R_o, R_d, S_o, S_d, etc.). Various new integrals are evaluated where needed using the computed values of s and p obtained above.

(Some of the expressions relate directly to those in Pucel's paper and do not appear in the Technical Report.)

2040-2240	Calculation of s and p (actually d) when no saturation occurs. Only I_d is printed for this case.
2250	Data

2.4 EXPERIMENTAL DETERMINATION OF PARAMETERS

This section describes how the FET devices are characterized. Three sets of measurements are made. These correspond to the three types of analysis performed using the FET modeling code. They include dc measurements, noise figure determinations, and small signal or S-parameter measurements. Three types of devices are included here: the NEC 38800, the Dexcel 2503A, and devices made at TRW. The NEC and Dexcel devices represent state-of-the art one-half micron FETs. The TRW device is a 1 micron device with an implanted channel.

To evaluate chip devices, they must be mounted in a fixture to which connections can be made. For this study the devices are mounted on Dexcel 50 ohm carriers. The carriers consist of two microstrip lines on an alumina dielectric which are separated by a metal ground bar. The devices are epoxied to the ground between the microstrip lines. Bond wires connect the gate and drain to the strip lines and the source to the ground bar for a common source configuration. The carrier is fastened in a U-shaped fixture made of gold plated aluminum, such that the microstrip lines terminate at holes in the fixture. Omni/spectra connectors (OSM 244-4ASF) are attached to the fixture with the center conductor protruding through the hole to make contact with the microstrip. Electrical contact is obtained with a pressure contact between the pin and stripline. The result is a compact fixture of 2.8 cm from connector to connector.

Using devices mounted in fixtures, the dc characteristics were measured. The Dexcel devices have saturation source-to-drain currents (I_{dss}) of between 25 and 45 mA. The NEC devices are more uniform with values of I_{dss} between 55 and 70 mA. The transconductance for both devices is between 25 and 30 mmho at 10 mA of drain current. The TRW devices have an I_{dss} of about 35 mA and a lower transconductance of about 20 mmho. The NEC and Dexcel devices are comparable. They both have a one-half micron gate. The NEC gate is 300 um wide while the Dexcel device is 275 um wide. This difference in width would explain the difference in I_{dss}. The TRW device has a 1.2μm gate that is 250 μm wide.

The transconductance can be found from Figure 2-10 in which drain current is plotted as a function of gate bias for a drain bias of 3 V. The transconductance is the slope of the lines. Data for NEC devices (closed symbols) fall very nearly on a single curve, demonstrating the uniformity in I_{dss} for the devices measured. Data for Dexcel devices (open symbols) fall along individual curves for different devices. The distribution results from the variation in I_{dss} for these devices. For all devices, the slope of the lines in the linear region is about 30 mmho. One TRW device is included for comparison. The transconductance is about 20 mmho, but it is not constant, even at low gate voltages.

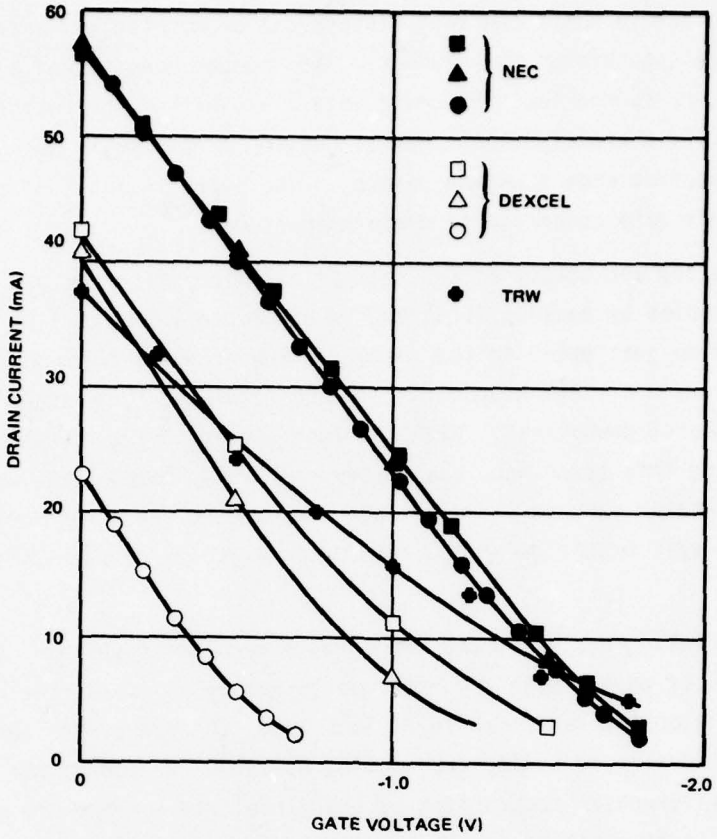


Figure 2-10. Drain Current vs Gate Voltage for NEC 38800, Dexcel 2503A, and TRW devices. Data is for a drain voltage of 3V and room temperature. The slope of the lines gives the device transconductance.

The noise figure measurements are made using an Ailtech Model 7380 system noise monitor and associated solid state noise generator. Device noise figures depend on impedances seen at the input and output. Stub or slide screw tuners must therefore be used at each port to allow one to tune the matching network for minimum device noise. Triple-stub tuners have sliding shortes in their legs and must be used outside the bias tees and device. Such an arrangement reduces the impedance range that can be tuned. As a result, the optimum noise match may not be obtained. To improve the tuning range, Microlab/FXR Model N311A slide screw tuners are used. These tuners are non-shorting and can thus be used inside the bias tees, next to the device fixture.

Temperature dependent noise figure measurements require a special system for cooling the fixture and device. The temperature-regulating system built for this study

consists of a chamber in which the test fixture can be mounted and associated hardware for flowing cooled gas through the chamber. The chamber consists of a rectangular box in which the fixture is mounted. RF power enters and exists the chamber through 3 cm lengths of semirigid stainless steel coaxial cable. O-ring seals are used around the cable to allow movement when changing devices. The overall length of the loaded chamber is about 12 cm from gate connector to drain connector.

Holes at the top and bottom of the chamber allow dry nitrogen gas to flow through. The gas flow is cooled by passing it through a copper coil immersed in liquid nitrogen. A heater in the flow just prior to the chamber allows the gas to be reheated to some intermediate temperature. The heater can also be regulated by feedback circuitry from a thermocouple located downstream. With the loop closed, improved temperature stability is obtained. Using this technique, device temperature is highly dependent on gas flow rate. Thus both heater current and flow rate are used to set the chamber temperature. Using the present system configuration, device temperatures between 300° and 140°K have been maintained.

Care must be taken when using the temperature regulating system. Before the chamber is cooled, it must be purged with dry nitrogen to remove any moisture. If moisture is allowed to condense on the device while it is biased, the device can short out. The device can also be destroyed during the cooling operation if one of the contacts opens up. Because of differential contraction of the dielectric carrier and other parts of the test fixture, it is possible for the pressure contact between the OSM center pin and the microstrip to open. Ordinarily, if either contact is suddenly opened, the device is preserved because the channel can safely support I_{dss}, the room temperature current. However, as the device cools, the value of I_{dss} increases. If the gate contact opens while the device is cooled, the resulting current will be larger than the room temperature I_{dss}. As a result, the channel may be destroyed.

Three measures are taken to protect the device and the experiment from an open contact when cooling. First, the device is cooled and warmed slowly to prevent rapid contraction and expansion of the fixture parts and connecting cables. Second, the drain power supply is current-limited to a value just above room temperature I_{dss}. Finally, the device is always gate biased to a current below I_{dss} when operated below room temperature. Taking these precautions prevents burning out the device and usually results in successful operation throughout the temperature range.

The temperature regulating system affects the noise measurement through the noise figure of the device, of course, and also through two effects related to the chamber cable and connections. First, additional losses are incurred due to the added line lengths of the semirigid cable and the added connector on each side of the device. These losses are accounted for by measuring the insertion loss of the chamber with a fixture containing a microstrip throughline and no device. The resulting

measured loss can be divided by 2 and appropriately entered into the noise figure calculation. The second effect of the cable connections is not as easily removed. The additional line length moves the tuners away from the device much as the bias tees do. The resulting configuration reduces the impedance range accessible with the tuners. Fortunately, the reduction in tuning range is not as severe for the cable lengths as it is for the bias tees since the bias tees contain more components than a single transmission line.

Using the system described, measurements of noise figure vs drain current, frequency, and temperature where made for the NEC and Dexcel devices. These measurements will be presented first. Then the more recent results for a TRW device will be given. The data for the one-half micron devices will illustrate the measurement technique and the type of behavior obtained for GaAs FETs.

A noise figure comparison for the NEC and Dexcel devices is shown in Figure 2-11. The noise figures are measured at 10 GHz and 295°K for a current range of 5 mA to I_{dss}

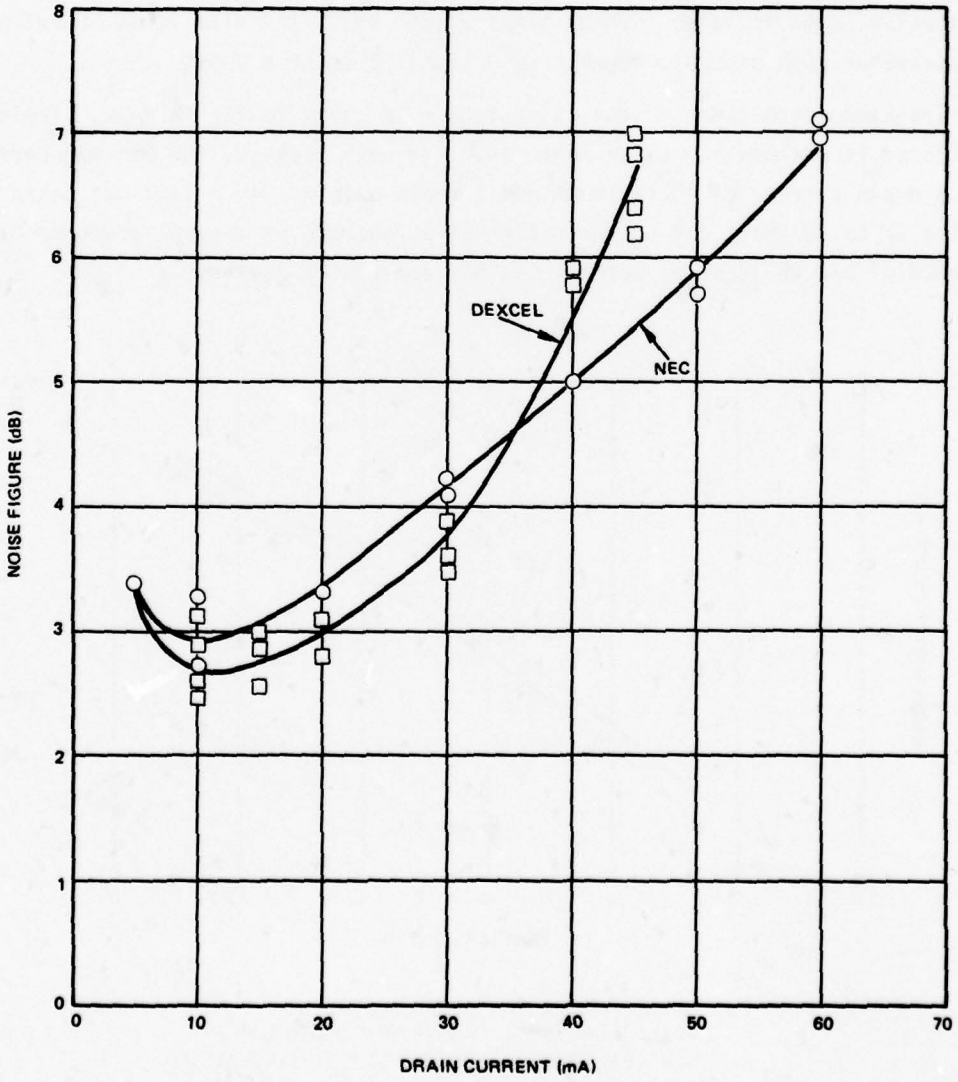


Figure 2-11. Noise Figure as a Function of Drain Current for Dexcel and NEC Devices. Data is for 10 GHz and room temperature.

for each device. The drain bias is 3 V. Such biasing operates both devices well into the saturated region. Each device has a minimum noise figure at a drain current of between 10 and 15 mA. For the NEC device, the minimum is about 2.9 dB. For the Dexcel device, the minimum is about 2.7 dB. Systematic errors such as reflections from connectors and the OSM/microstrip interfaces limit the accuracy of comparisons between devices to differences greater than ao but 0.3 dB. Therefore, the minimum noise figure for the two devices is not significantly different.

The scatter in the data for a given device and bias point occurs for two reasons. First, the measured noise figure depends on the proper impedance match being achieved between the 50 ohm system and the FET. A particular input and output impedance exists which reslults in a minimum noise figure. Thus differences in measured noise figures reflect a less than optimum impedance match for the larger values. The second reason for measuring different values at the same point relates to the accuracy of the system noise monitor. The digital readouts do not allow precision within 0.25 dB. To overcome this limitation, data is taken several times at one point and also taken as a function of some parameter such as drain current to allow fitting of a smooth curve.

The frequency dependence of the noise figure is shown in Figure 2-12. The noise figure plotted is the minimum value measured. For both devices, the minimum corresponds to a drain current of 10 to 15 mA and a drain bais of 3 V. Data was taken at frequencies up to 10 GHz. The curves represent an average of several measurements. A difference of 0.2 dB is shown between the NEC and Dexcel devices.

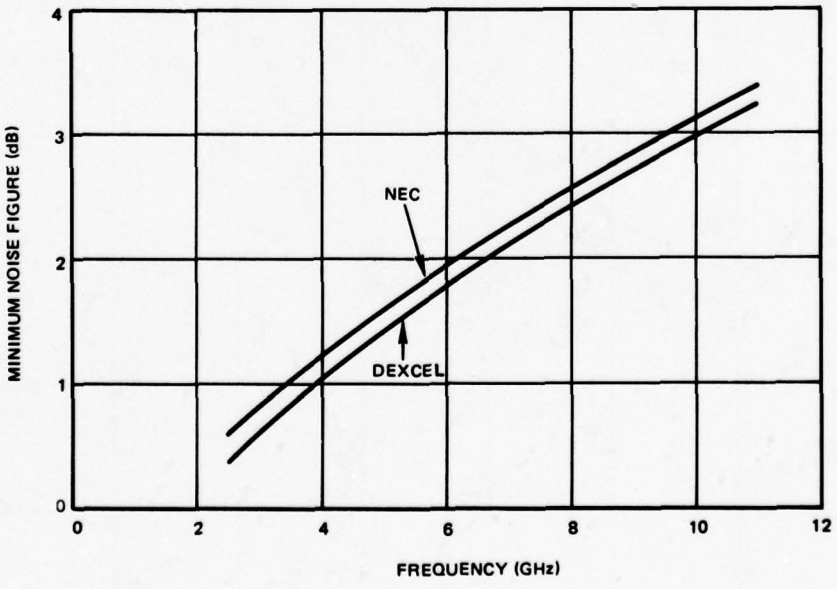


Figure 2-12. Noise Figure vs Frequency for NEC and Dexcel Devices. Measurements are for devices at room temperature biased at 3V drain voltage and 10 mA drain current.

The results of device cooling are presented in the following series of figures. In Figure 2-13, th noise figure is plotted vs the drain current for a Dexcel device. Data at four temperatures are included. The general current dependence of the noise figure does not change as the device is cooled. However, the magnitude of the noise figure is reduced at all bias points as the temperature is reduced. In addition, the minimum appears to move toward higher drain currents with cooling. This observation may be connected with the increase in I_{dss} that occurs as the temperature is reduced. Notice that because the minimum becomes broader at low temperatures, a bias point of 10 to 15 mA always results in the lowest noise operation regardless of temperature.

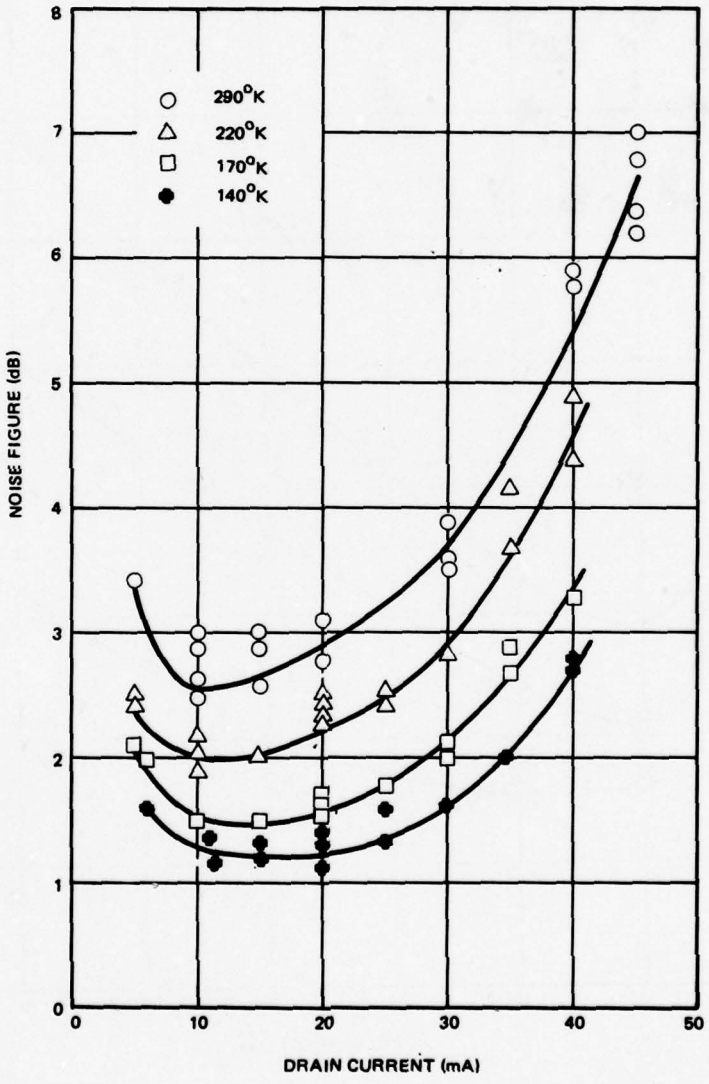


Figure 2-13. Noise Figure vs Drain Current as a Function of Device Temperature. Device is a Dexcel 2503A biased at 3V drain voltage. The frequency is 10 GHz.

Figure 2-14 is a similar plot for an NEC device. The minimum noise figure is reduced from 3 to 1.5 dB by cooling the device from room temperature to 150°K. The Dexcel device of Figure 2-13 also shows a noise figure reduction by a factor of 2 when cooled from room temperature to 140°K.

Data for a second Dexcel device is shown in Figure 2-15. As noted earlier, I_{dss} for the Dexcel devices ranges from 25 to 45 mA. The device of Figure 2-13 represents one of the upper limit devices. The device of Figure 2-15 was chosen as a representative of the lower part of the range of devices. The temperature-dependence of the noise

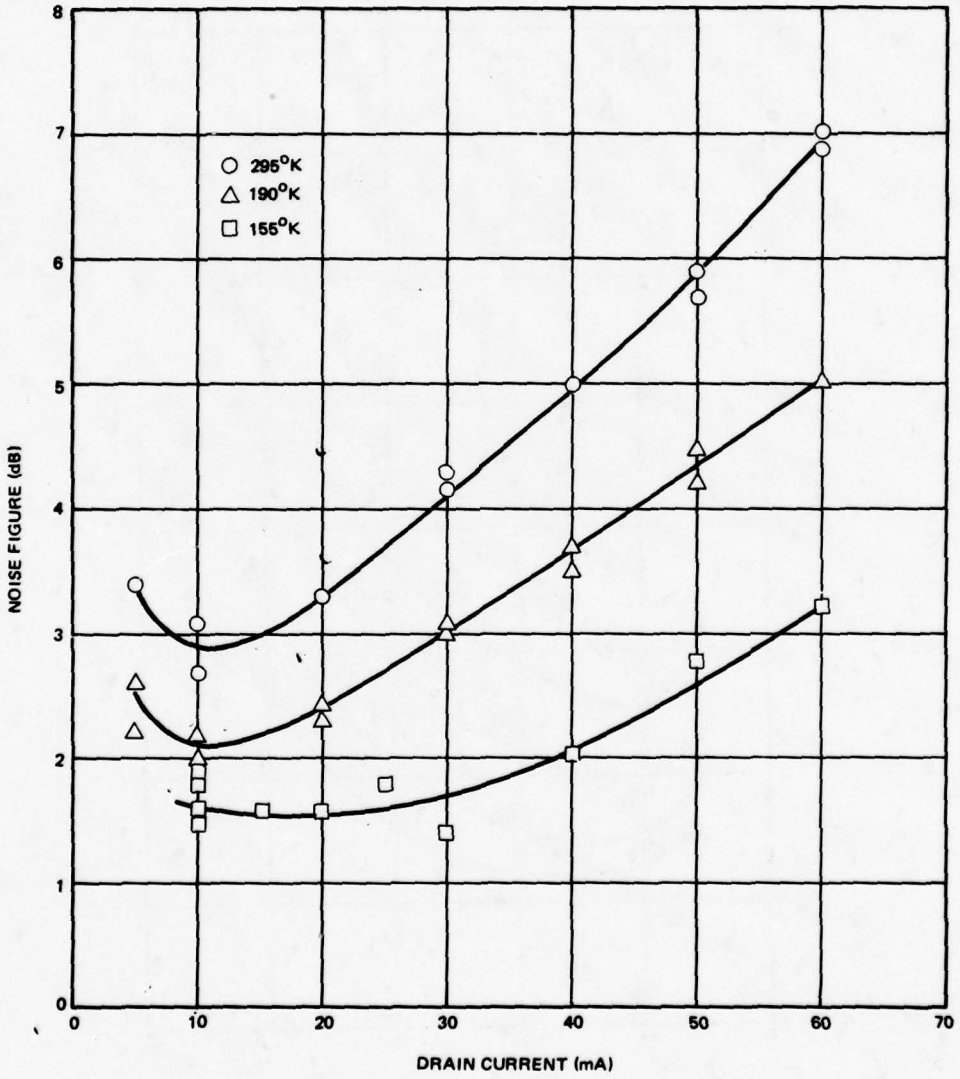


Figure 2-14. Noise Figure vs Drain Current as a Function of Device Temperature. Device is an NEC 38800 biased at 3V drain voltage. The frequency is 10 GHz.

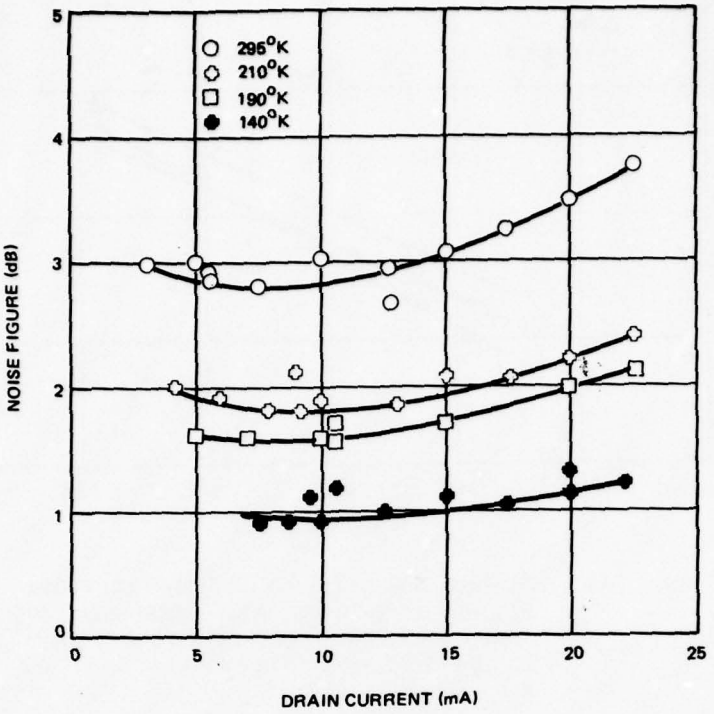


Figure 2-15. Noise Figure vs Drain Current as a Function of Device Temperature. Device is a low I_{dss} Dexcel 2503A biased at 3V drain voltage. The frequency is 10 GHz.

figure is similar to that of the previous Dexcel device and the device seems to have a weaker noise figure dependence on drain current. The difference is only illusionary, however. Consider the data of Figure 2-13 over the limited range of 5 to 25 mA. The rate of increase of noise figure with current is about the same for both devices. For example, at room temperature the increase in noise figure above the minimum at 25 mA is about 1 dB in Figures 2-13 and 2-15. One could explain the results as the result of two similar devices having different built-in potentials and therefore different values of I_{dss}.

To summarize the temperature-dependent data, the minimum noise figures of the last three figures are plotted as a function of temperature in Figure 2-16. In the figure, Dexcel, NEC, and Dexcel 2 refer to the devices of Figures 2-13, 2-14, and 2-15, respectively. The data generally fall along straight lines with slopes of 0.009 to 0.011 dB/°C. The range of noise figures is such that coverting the values from dB to absolute ratios and plotting the ratios against temperature still gives straight lines. One may conclude that between 150 and 300°K, the device noise figure is proportional to temperature.

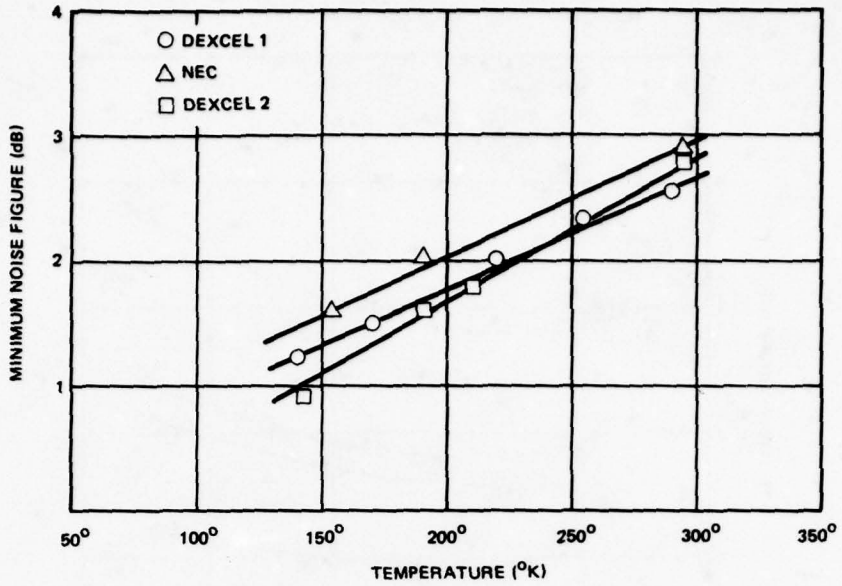


Figure 2-16. Minimum Noise Figure of Previous Three Figures as a Function of Temperature. "Dexcel 1", "NEC" and "DEXCEL 2" refer to the devices of Figures 2-4, 2-5, and 2-6, respectively.

Device gain is also measured with the Ailtech system noise monitor. Figure 2-11 indicated the noise figure dependence on drain current for the two types of device. Figure 2-17 shows the gain associated with those noise figures. Both devices have a peak associated gain of 4.5 to 5 dB. The maximum gain occurs at drain currents above the point of minimum noise. Low noise operation occurs at drain currents of 10 to 15 mA. Gain is a maximum in the 20 to 30 mA range.

Figure 2-18 shows the temperature dependence of the gain. The square symbols refer to measurements on a Dexcel device. The round symbols refer to an NEC device. Because gain is a function of drain current, as seen above, data for two values of drain current are plotted in Figure 2-18. The open symbols refer to 10 mA of drain current and the closed symbols to 15 mA. This current range corresponds to minimum noise figure bias conditions. The lines sketched through the Dexcel device data indicate that a 0.6 dB increase in gain occurs when the drain current is increased from 10 to 15 mA. This increase is independent of temperatue. In addition, the gain increases as the device is cooled.

From noise figure and associated gain, the noise measure, M, can be calculated. This figure of merit describes the noise figure contribution of one stage in an infinite cascade of stages. Therefore, M is a useful measure of suitability for amplifier use. In Figure 2-19, M is calculated and plotted as a function of drain current for an NEC and Dexcel device. For high drain currents, the NEC device has a better figure of merit. At low drain currents, M is about the same for both types of device. This result reflects the similarity in noise figure and associated gain for the two devices.

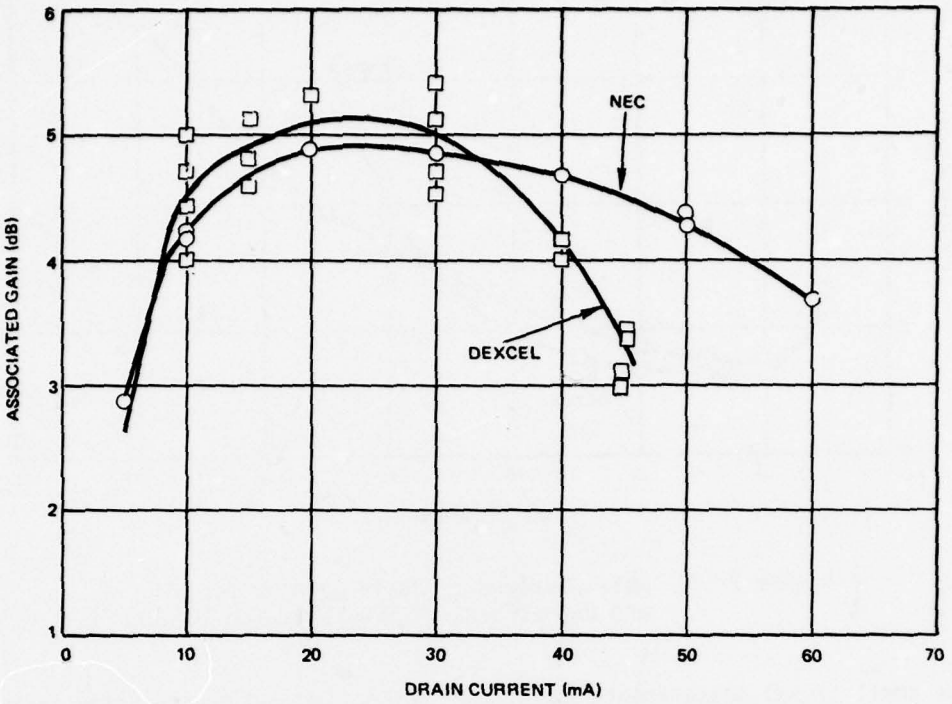


Figure 2-17. Gain Associated with Noise Figures of Figure 2-11. Devices are at room temperature and operated at 10 GHz.

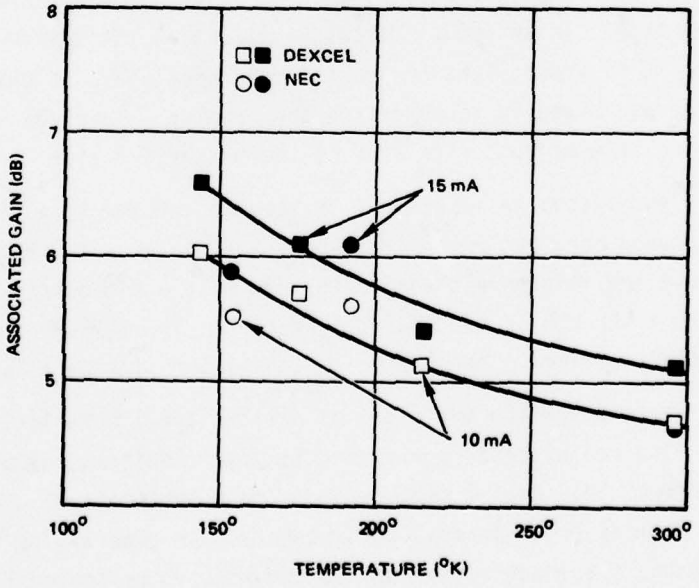


Figure 2-18. Associated Gain vs Temperature for Measurements at 10 GHz and Drain Bias of 3V. Square symbols refer to a Dexcel 2503A device. Round symbols refer to an NEC 38800 device. Open symbols are for gain at 10 mA drain current. Closed symbols are for gain at 15 mA.

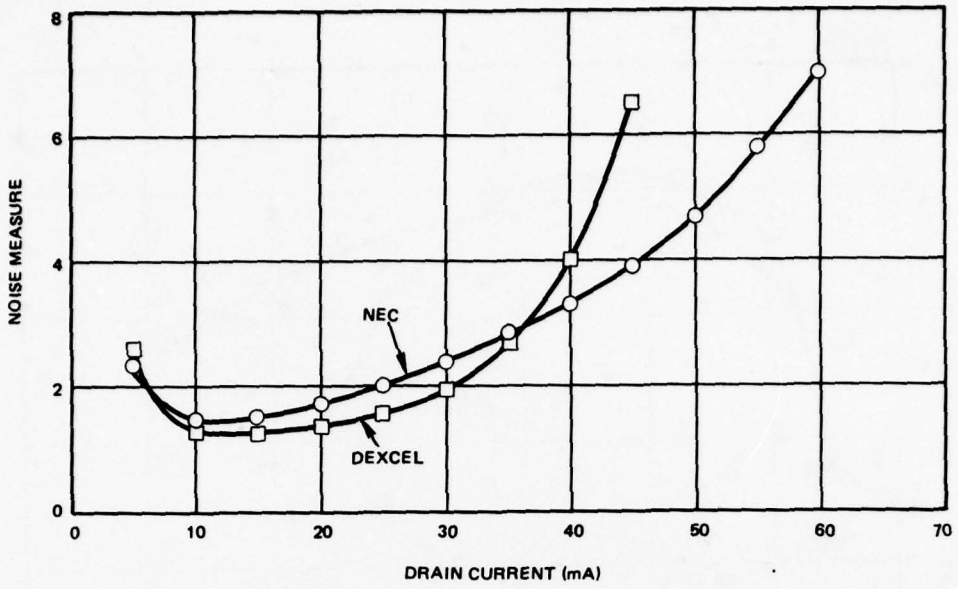


Figure 2-19. Noise Measure vs Drain Current for NEC and Dexcel Devices. Data is for 10 GHz.

The small signal measurements consist of reflection and transmission tests expressed in terms of S-parameters. The S-parameters of a device are useful for circuit design at microwave frequencies. The reflection measurements depend upon providing an effective short at a plane corresponding to the input or output of the device. For a chip device which must be bonded into a carrier, one may either attempt to set the referrence plane at the device itself or at the end of the bond wires which connect the device to the microstrip. In an actual circuit application the device will be connected with bond wires, so it is appropriate to set the reference plane at the end of the bond wires. Care must be exercised in interpreting the results. They are strictly valid only for the type and size of bond wire used on the measured device.

The short used for system calibration is a regular carrier in a fixture. No device is mounted on the ground bar, but rather the space between ground and microstrip is filled in with metal to move the reference plane to the end of the microstrip. For the transmission measurements a through is used for calibration. The through consists of a normal fixture with a special carrier. The carrier is fabricated similar to a regular carrier,

Measured S-parameters for the two types of devices are listed in Table 2-7 for three frequencies. The measurements correspond to bias conditions of 3 V drain voltage and 10 mA drain current. All measurements are for room temperature. The input relfection parameter S_{11} decreases for increasing frequency. In general, as S_{11} decreases it becomes easier to match the input of the device for minimum reflected loss. The forward transmission parameters, S_{21}, also decrease as frequency increases. Therefore, the maximum available gain is reduced at higher frequencies. The last column of Table 2-7 lists the computed stability factor, K. If K is greater than one, the device is unconditionally stable at that frequency. Both types of devices are unconditionally stable at 10 GHz. However, at lower frequencies, one must match the device properly to

assure stability. From a consideration of stability, one would conclude that the Dexcel device is easier to design with because it is nearly stable at all frequencies in the measured range.

In low noise amplifier design, it is necessary to adjust the input and output matching networks to provide a compromise between low noise and required gain. The maximum attainable gain for the two devices is listed in Table 2-8. The gain listed is the maximum available gain (MAG) if the device is inherently stable, or the maximum stable gain (MSG) if the device is not unconditionally stable. MSG is the gain that would be obtained if the input and output matching were adjusted such that K = 1. From the table one may conclude that the NEC device is capable of providing more gain than the Dexcel device if noise figure is not of primary concern.

The S-parameters measured for a device determine the impedance matching required for maximum power transfer and power gain. For low noise amplifiers, the devices, particularly the input stage device must be matched for optimum noise figure, not for optimum gain impedance (S_{11} and S_{22}). To measure the optimum source and load impedances for low noise, the slide screw tuners are reset to the positions for which lowest noise was measured. Then a network analyzer is used to measure their impedance with the opposite port terminated in 50 ohm to simulate their environment during testing.

Table 2-9 lists the optimum source and load impedances for minimum noise as measured for the two types of devices. The measurements are for 10 GHz operation. Notice that the Dexcel device's optimum low noise input impedance is about the same as the optimum high gain impedance (S_{11} of Table 2-7). The remaining three impedances of Table 2-9 are lower than the corresponding high gain values. The values listed are for room temperature. However, very little change in tuner position is required to optimize the noise at lower temperatures. The required change in magnitude of matching impedance would never be more than ± 0.05.

Figure 2-20 gives noise figure as a function of drain current for a TRW device. Noise figures are shown for 4 and 10 GHz. The spread in data around the minimum at 10 mA indicates several different tuner settings at 10 GHz. The minimum noise figure is about 1.9 dB at 4 GHz and 4.8 dB at 10 GHz. The device shown has a 1.2 um gate. The gain associated with the noise figure for the device is plotted in Figure 2-21. The maximum associated gain occurs at about 25 mA. At 4 GHz the gain at minimum noise (10 mA) is 6.5 dB. At 10 GHz the gain associated with the minimum noise figure is 2 dB.

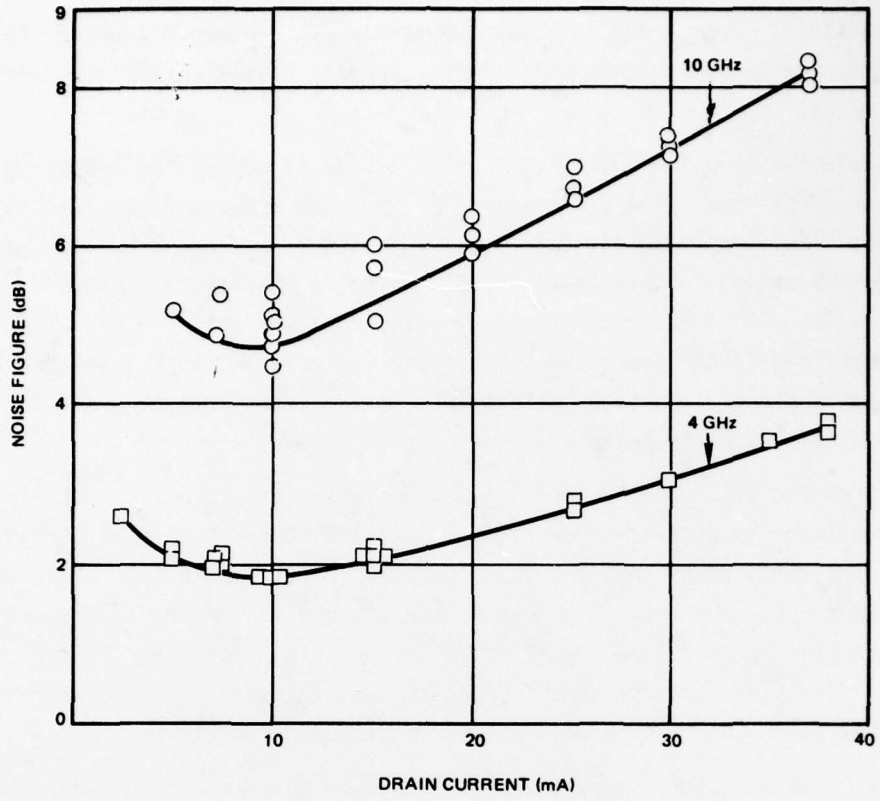


Figure 2-20. Noise Figure vs Drain Current for a TRW Device with a 1.2 μm Gate

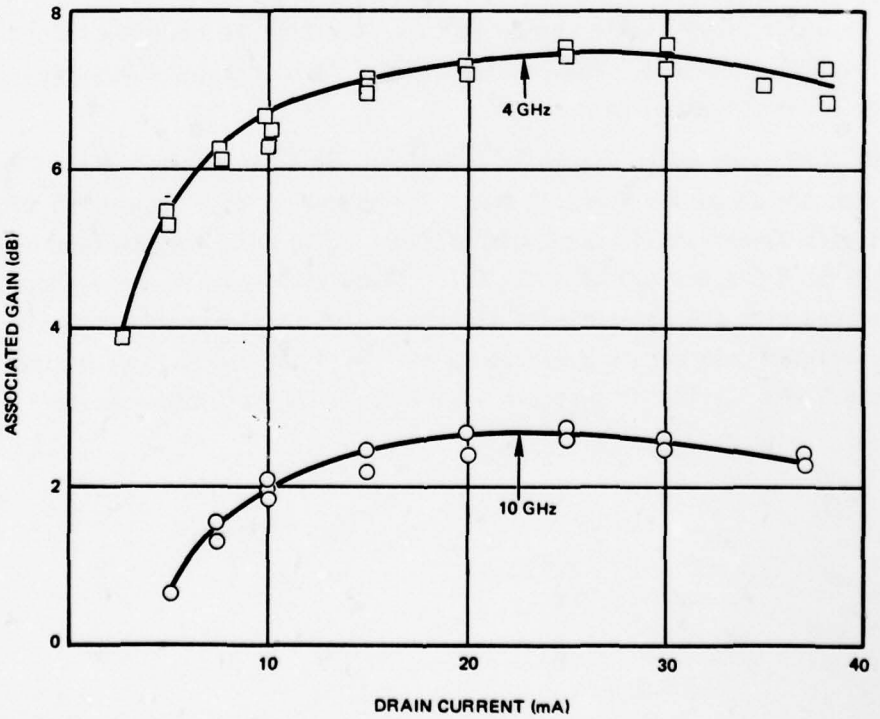


Figure 2-21. Gain Associated with the Noise Figures for the TRW Device of Figure 2-20

Table 2-7. S-parameter measurements for Dexcel 2503A and NEC 38800 devices at room temperature. Measurements include the effects of bond wires.

f_1 (GHz)	S_{11}	S_{21}	S_{12}	S_{22}	K
	(magnitude) (angle in degrees)				
	DEXCEL				
3	.64 -26	2.6 143	.032 71	.72 -34	1.7
6	.63 -90	2.2 107	.063 43	.78 -32	0.90
10	.42 -142	1.6 74	.032 93	.81 -56	2.5
	NEC				
3	.91 -26	2.0 156	.032 80	.73 -28	0.43
6	.86 -60	1.9 130	.045 59	.72 -36	0.62
10	.75 -94	1.4 102	.032 94	.72 -57	1.8

Table 2-8. Maximum obtainable gain as calculated from the S-parameters of Table 2-7. "MAG" is maximum available gain. "MSG" is maximum stable gain.

f_1 (GHz)	Gain (dB)	Type
	DEXCEL	
3	14.2	MAG
6	15.4	MSG
10	10.3	MAG
	NEC	
3	18.0	MSG
6	16.3	MSG
10	11.1	MAG

Table 2-9. Optimum source and load impedance for low noise operation of Dexcel 2503A and NSEC 38800 devices.

Device	Optimum Source Impedance	Optimum Load Impedance
	(magnitude) (angle in degrees)	
DEXCEL	.45 -110	.35 -150
NEC	.25 -150	.50 -110

2.5 COMPARISON OF MODEL TO EXPERIMENT

With the experimental data just presented, it is possible to evaluate the accuracy of the FET model. First consider the TRW device of Figures 2-20 and 2-21. The IV curves for the device are shown in Figure 2-22. The measured data is shown with solid lines at various values of gate voltage. The open symbols represent the values obtained from the FET model. The excellent agreement is the result of some fitting of the device parameters. To fit the IV curves, one can adjust the channel depth a, doping density N, source resistance R_s, and drain resistance R_d. For this particular device, a = 0.185 μm and N = 1.2×10^{17} atom/cm^3. The value used for the source resistance is 10 ohms, which is about the value aimed for in device fabrication. The value of R_s is the same as that obtained by fitting the S-parameters to the equivalent circuit.

Because the FET model does not include the effects of depletion beyond the gate region, the drain resistance is modeled as

$$R_d = a + b\,|V_{gg}|$$

for calculation of the dc curves. The fit shown in Figure 2-22 was obtained for a = 20 ohms and b = 10 ohms/V. The magnitude of these values indicates that the channel is partially depleted in the region between the gate and the drain. This depletion affects the amount of current that flows for particular bias conditions and is, therefore, important when computing the dc characteristics. However, the drain resistance has no direct contribution to the noise figure. It has only an indirect effect through the drain current. As a result, the noise figure is relatively insensitive to the form of the drain resistance.

Using the parameter values obtained from the dc analysis, the noise figure can be obtained. Figure 2-23 consists of the output from OPTION1 for the device at 4 GHz. The noise figure is computed as 1.8 dB for a drain current of 12 mA. The noise figure obtained using the Fukui equation is 2.0 dB. From Figure 2-20, one observes that the measured noise figure is about 2 dB. The agreement among the three values is due to two additional parameters. First, the gate resistance, R_g, of 4 ohms is chosen because it provides the proper noise figure using the Fukui formulation. R_g has not been measured for the device. Fitted S-parameter data indicates that a value of 2 ohms for R_g is expected. Using a value of 2 ohms for R_g would reduce the calculated noise figures by about 0.1 dB. Such a change would still produce acceptable agreement between the measured and calculated values of noise figure.

The second adjustment made is to the value of the diffusion constant, D. The value of D used is 60 cm^2/sec as indicated by DIFCON in the section of Figure 2-23 containing additional parameters. Because D is adjusted to fit the data at 4 GHz, the validity of the model is not shown. However, the usefullness of the TRW model can be shown if the

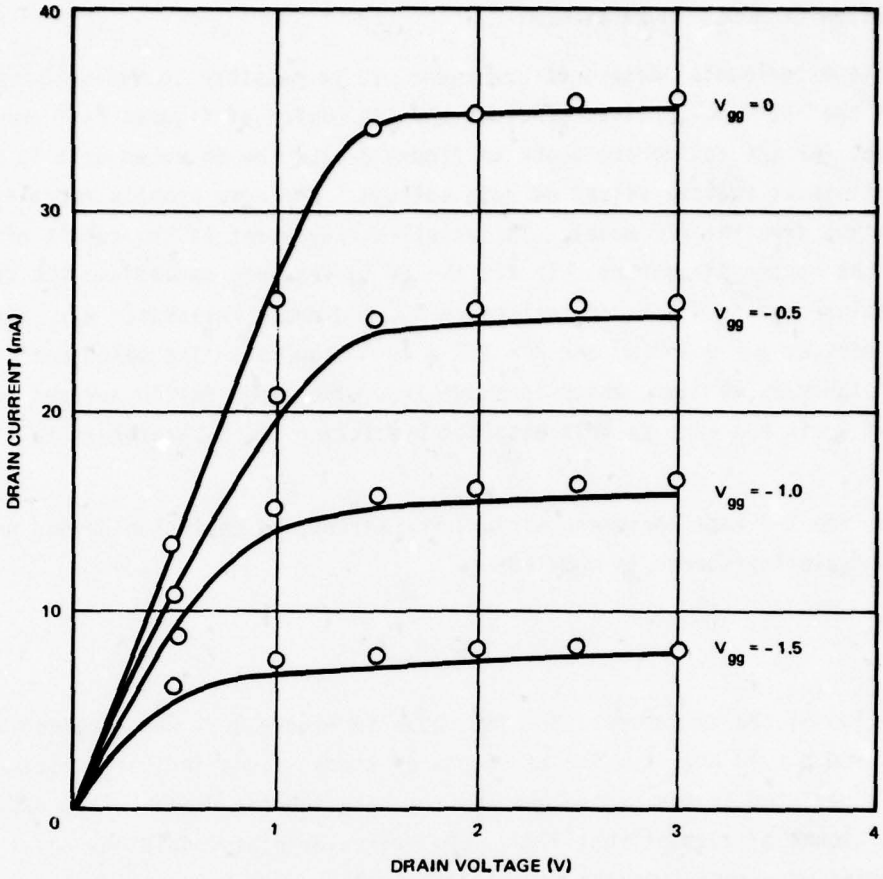


Figure 2-22. Drain Current vs Drain Voltage for a TRW Device. Solid curves are obtained from experimental data. The circles are calculated from the FET model.

model now gives the proper noise figure under different conditions such as when measured at 10 GHz. Figure 2-24 is another OPTION1 listing at 10 GHz using the identical parameters from Figure 2-23. The FET modeled noise figure is now 4.5 dB which compares quite well with the measured noise figure shown in Figure 2-20. The noise figure calculated using the Fukui empirical equation is 3.9 dB. The noise figure from the Fukui equation is somewhat low due to the fact that no second order frequency terms are included. The TRW model includes second order terms. These are important because the device cutoff frequency is about 13 GHz.

Next, data for a Dexcel device will be compared with the model. The device to be considered is that of Figure 2-15. From the dc analysis, the following parameters are assumed: a = 0.12 μm, N = 1.5 x 10^{17} atom/cm^3, R_s = 3.6 ohms, and R_d = 20 ohms. The Dexcel 2503A is a one-half micron device. The validity of the origional Pucel model has not been established for such short gate devices. Initial attempts to fit the model

to such devices indicate that the calculated noise figures are too small. One reason for this discrepancy has already been discussed. The high field diffusion constant which was adjusted to a value of 35 cm^2/sec for 2 μm devices is probably larger for shorter devices. Increasing D changes two features of the computed noise figure. First, it increases the overall magnitude of the noise figure. Second, increasing D increases the slope of the noise figure vs drain current for currents above the minimum.

Because the value of the high field diffusion constant is not clearly defined, one can adjust its value to fit experimental data. However, if D is increased until the experimental and calculated noise figures match at, for example, the point of minimum noise figure, the resulting slope of the noise figure vs I_d durve is too steep. The discrepancy in slope occurs primarily for the short gate devices. A reason for the discrepancy has been found in the origional analysis of the noise figure. Figure 4-1 of Appendix A shows the equivalent circuit for which noise generation is computed. The circuit contains just one capacitor, the source-to-gate capacitance C_{sg}. C_{sg} is computed from the change in charge on the gate to the voltage applied to the gate. The circuit does not include a capacitance between the source and gate or the gate and drain due to the physical proximity of these pairs of metal layers. In the original derivation, these two capacitances, C_{sw} and C_{gd}, respectively were not included because they are small in comparison to C_{sg}. However, for short gate devices, the electrodes are much closer together and the capacitance does make a significant contribution to the total noise figure of the device.

Figure 2-25 shows noise figure data at two temperatures for a low I_{dss} Dexcel device. The solid curves represent the model predictions with the inclusion of the C_{sw} and C_{gd} contributions. The solid lines result from values of $C_{sw} = C_{gd} = 0.032$ pF as calculated in ANCIL. The slope and magnitudes of the noise figures then match at large currents for D = 50 cm^2/sec and at 300°K. Using the same parameters, the predicted noise figure at 140°K is also in general agreement with experiment.

The revision of the value for D and the inclusion of C_{sw} and C_{gd} have improved the agreement between model and experiment for short gate devices. The model is still incomplete, however. As can be seen by the prediction for noise figure at 300°K in Figure 2-25, the model no longer predicts the minimum as it did for longer gates. The dashed line in the figure which does fit the 300°K data was obtained by decreasing D and increasing C_{sw} and C_{gd}. Although the resulting values are unrealistic, the result does indicate the direction for further investigations and refinements of the model.

```
RUN 31   KU FET-2 1   SUMMARY AT 4 GHZ

GATE LENGTH      =   1.20 MICRONS          VGG =  -1.25 V
GATE WIDTH       = 250.00 MICRONS          VDD =   3.00 V
CHANNEL DEPTH    =    .185MICRONS          RSG =  10.00 OHMS
DOPING DENSITY   = 1.15E+17 ATOMS/CC       RGD =  20.00 OHMS
DEVICE TEMP      = 300.00 K                RGATE =   4.00 OHM
FREQ.            =   4.00 GHZ

          NF(FUKUI) = 1.965 DB
       NOISE FIGURE =  1.8286 DB
   TRANSCONDUCTANCE = 19.78   MMHO
      TERMINAL GM   = 16.51   MMHO
 CUT-OFF FREQUENCY  = 12.80   GHZ

CAPACITANCE (PF)                          RESISTANCE (OHM)
                    INTRINSIC
CSG = .2442                               RI (GATE CHARGE) =    9.83
CGD = .0299                                    RD (OUTPUT) = 4597.39
                    PARASITIC
CSD = .0397                               RM (GATE METAL) =    4.00
                                               RS (SOURCE) =   10.00
                                               RDR (DRAIN) =   20.00

   REGION 1                                   REGION II
 L1 =  .614 MICRON                         L2 =  .586 MICRON
    = 51.15 %                                 = 48.85 %
  S =  .8484+200                            D =  .8903430

                ADDITIONAL PARAMETERS
 ID = -12.15 MA                              IS =-101.56 MA
WOO = -2.649 V                              PUT =  -.679 V
 GO = -1.401 MMHO                        SATDEX =  -.122
 ES =  2.900 KV/CM                          MUO = 4110.0 CM2/V/SEC
 VS = 1.19E+07 CM/SEC                     DIFCON =   60.0 CM2/SEC
                                           DIFIC =  1.107 PF/CM

S11:    .923    < -36.7      S12:    .069    <  69.0
S21:   1.475    < 146.7      S22:    .953    < -13.1
OPTIMUM SOURCE   .891  <  20.2      OPTIMUM LOAD   .667  <  20.0
```

Figure 2-23. Output Using OPTION1 for a TRW Device Showing the Calculated Noise Figures at 4 GHz

```
RUN 32   KU FET-2 1   SUMMARY AT 10 GHZ

GATE LENGTH      =   1.20 MICRONS          VGG =  -1.25 V
GATE WIDTH       = 250.00 MICRONS          VDD =   3.00 V
CHANNEL DEPTH    =    .185MICRONS          RSG =  10.00 OHMS
DOPING DENSITY   = 1.15E+17 ATOMS/CC       RGD =  20.00 OHMS
DEVICE TEMP      = 300.00 K                RGATE =  4.00 OHM
FREQ.            =  10.00 GHZ

          NF(FUKUI) = 3.857 DB
        NOISE FIGURE =  4.4663 DB
   TRANSCONDUCTANCE = 18.72   MMHO
          TERMINAL GM = 16.51   MMHO
  CUT-OFF FREQUENCY = 12.89   GHZ

CAPACITANCE (PF)                        RESISTANCE (OHM)
                  INTRINSIC
CSG = .2442                             RI (GATE CHARGE) =    9.83
CGD = .0299                               RD (OUTPUT) = 4597.39
                  PARASITIC
CSD = .0397                             RM (GATE METAL) =    4.00
                                          RS (SOURCE) =   10.00
                                          RDR (DRAIN) =   20.00

   REGION I                               REGION II
 L1 =  .614 MICRON                        L2 =  .586 MICRON
    = 51.15 %                                = 48.85 %
  S =  .8484290                              D =  .8903430

                ADDITIONAL PARAMETERS
 ID = -12.15 MA                          IS =-101.56 MA
WOO = -2.949 V                          PHI =  -.679 V
 GO = -1.401 MMHO                     SATDEV =  -.122
 ES =  2.900 KV/CM                       MUO = 4110.0 CM2/V/SEC
 VS = 1.19E+07 CM/SEC                  DIFCON =   60.0 CM2/SEC
                                        DIFIC =  1.107 PF/CM

S11:    .725    < -76.5     S12:    .123    <  40.9
S21:   1.066    < 110.4     S22:    .887    < -28.1
OPTIMUM SOURCE   .735 <  46.3     OPTIMUM LOAD   .737 <  32.2
```

Figure 2-24. Output Using OPTION1 for the Device of Figure 2-23 Showing the Calculated Noise Figures at 10 GHz

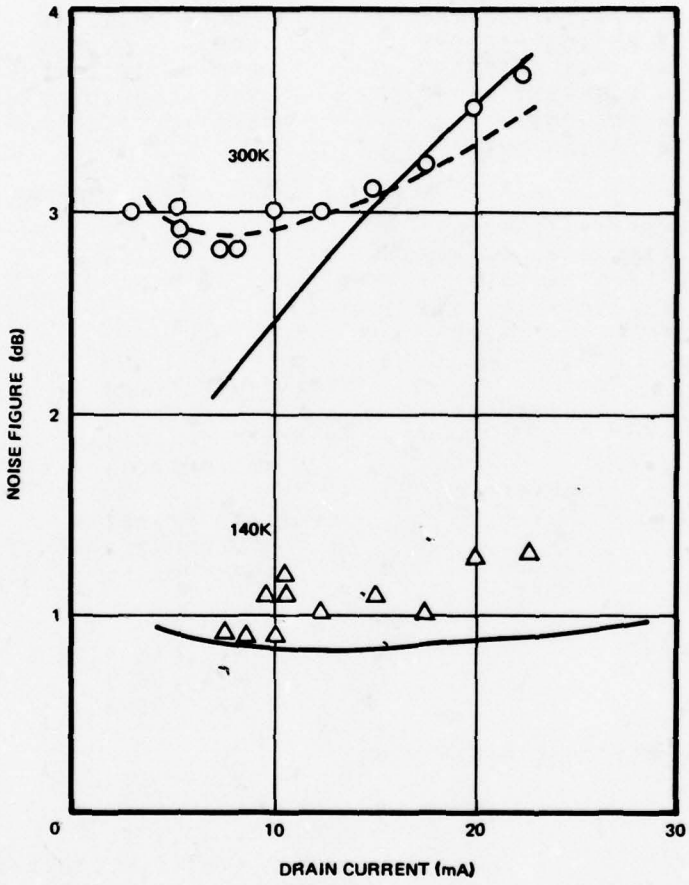


Figure 2-25. Noise Figure vs Drain Current for a Dexcel 2503A at 10 GHz. Solid lines represent model predictions. Dashed line is described in text.

3. INTEGRATED CIRCUIT MODELS

The purpose of this task as defined in the program statement of work was to incorporate the device models into SPICE, a commercial CAD program. This was accomplished. The FET model was also incorporated into COMPACT, a CAD program which is in common use for microwave circuit design.

3.1 SPICE

SPICE performs four analysis routines of interest to this program: small signal, large signal, Fourier, and transient. The small signal analysis is used for checking RF circuit performance. The large signal analysis is used for checking dc biasing. The transient analysis is used in oscillator design and to check on circuit stability, and the Fourier analysis is used to study distortion and intermodulation. In order to use the small signal and transient analysis routines, once must provide SPICE with a small signal equivalent circuit model of the active device. This is input either from a data file created by the device model or entered directly by hand from the device model output.

It can be seen either in Section 2 or in Appendix B that this capability has been made part of the FET model, and was discussed above. There were initially some discrepencies between the gain predicted for amplifier test cases by the small signal and transient analysis modes of SPICE, but this has been traced to a software problem in TRW's particular version of SPICE rather than a model problem. This has been resolved.

A more interesting problem was to create an appropriate large signal model for SPICE. While the FET model does accurately predict dc IV characteristics, its form would be very difficult to use with SPICE. Instead, a simpler large signal model was derived and was found to be of a form that the standard JFET model in the SPICE library could be adapted for large signal and Fourier analysis. The derivation appears in the first few pages of Section 5.3, and an example of the Fourier analysis applied to the analog multiplier is given in the computer printout in Appendix D.

3.2 COMPACT

Previous experience with SPICE in the silicon RF-LSI program led to some reservations about using it for microwave circuit designs, particularly when tuned matching elements are to be used. Basically, SPICE uses an equivalent circuit model, the correctness of which can't be directly measured. On the other hand, COMPACT uses device S-parameters and these are measured routinely. Further, COMPACT has optimization routines which allow selection a circuit topology, and starting element values. COMPACT will optimize the element values in accordance with several weighting functions on gain, bandwidth, etc.

The creation of the S-parameter data files for COMPACT is also shown in Section 2 and Appendix B. A particular example of interaction between the FET model and COMPACT for amplifier performance analysis is detailed in Section 5.2. That amplifier and a number of other test circuits were extensively analyzed on both SPICE and COMPACT. The correlations achieved between the two CAD programs was quite good, reflecting good correlations between the FET equivalent circuit model and the S-parameters.

There is little more to be said about this task other than the fact that it was completed and has been used extensively in the circuits technique studies described in Section 5.

4. PROCESSING TECHNOLOGY DEVELOPMENT

The overall objective of the GaAs RF-LSI program is the development of a number of analog building block circuits and the combination of those circuits into a monolithic LSI X-band receiver. While TRW has on previous programs developed small scale GaAs integrated circuits, several key improvements in processing technology were required to meet the goals of this program. Previous circuits relied upon 1.5 to 2.0 micron lithography, used mesa isolation techniques, and used the same doping concentration for all active devices. To satisfy the goals of this program, high yield one micron photolithography is required: one micron gates are needed for device performance and high yield so that functioning circuits at the LSI level can be realized. The primary source of yield loss associated with one micron gates is in the transition area down the mesa sides. This implies that a fully planar approach which does not rely on mesa isolation must be developed. Further, if one is to approach anything close to optimum circuit performance, there must be the flexibility of choosing different doping concentrations and profiles in accordance with the device type (FET or TED) and application (amplifier, analog multiplier, oscillator, etc).

These considerations mandate a multiple-ion implant technology, a significant advance over previous processing approaches. This is not to imply that the previous technologies are rendered useless; indeed, this development was a necessary precursor to a fully planar processing technology, and in fact many of the previously developed tools carry over directly into this program. This section starts with a discussion of the basic processing technologies which have served as a foundation for the new development work done on this program. After establishing this background, the discussion turns to the new processing tools developed for the GaAs RF-LSI circuits. These new tools are primarily in the area of ion implantation. A third section presents a summary of the results achieved to date. While the data presented in this section is in summary or sample form, a great deal more data is presented in the associated appendix, Appendix C.

4.1 BASIC TECHNOLOGIES

This section describes the epitaxial technology, ion implantation technology, and the processing technologies developed at TRW prior to the program inception. These technologies were instrumental in the development of our early GaAs nonimplanted monolithic circuits, and served as the starting points for this program. The epitaxial technology includes the deposition of semi-insulating layers as well as doped layers with various doping concentrations. The ion implantation had been explored earlier primarily for ohmic contact improvement, and a small number of implanted FETs were fabricated. However, the major ion implant development activity has been conducted during this program. The key improvements in these technologies as related to this program are described in detail in Section 4.2.

4.1.1 Epitaxial Technology

GaAs epitaxial layers are required for fabricating the TED active channel and for FET improvements. Further, epitaxial buffer layers will be used with all epitaxial active alyers and in the ion implant process rather than direct implant into Cr-doped substrates, for more repeatable device characteristics. The TEDs require a doping concentration in the range of 1-3 x $10^{16}cm^{-3}$ and a layer depth of $\approx$1 μm. These parameters are achieved best with epitaxial deposition.

FETs for low noise application may require low doping concentration under the gate and higher concentrations in the source-to-gate region. These low concentrations are achieved more readily by epitaxial depositions, although preliminary results suggest that ion implant into buffer layers may give adequate control at lower peak doping concentrations rather than direct implant into Cr-doped substrates. Therefore epitaxial buffer layers may be used to enhance the capability for low concentration ion implantation, and as a means for substituting for poor quality substrates.

Since 1974, gallium arsenide epitaxial layers have been fabricated at TRW by chemical vapor phase deposition (CVD) using arsine, gallium, and hydrogen chloride as the reactants. These layers have spanned an N-type carrier concentration range of 3 x $10^{12}cm^{-3}$ to 4 x $10^{18}cm^{-3}$. The lower concentrations are achieved without intentional chromium or oxygen dopants while the higher doping concentrations are achieved using a sulfur dopant from H_2S. TRW generally uses two epitaxial reactors for depositing the epi materials: one for high resistance buffer layers and the other for doped active layers.

The epitaxial deposition reactor is a vertical arsine-hydrogen chloride system as shown in Figures 4-1 and 4-2. The wafer is heated with a five-zone resistance heated furnace where zone one preheats the entry gases and zone two maintains the Ga reservoir at the desired temperature. Zone four is the region where epitaxial layer deposition takes place, while zone three and zone five are buffer zones for temperature stabilization.

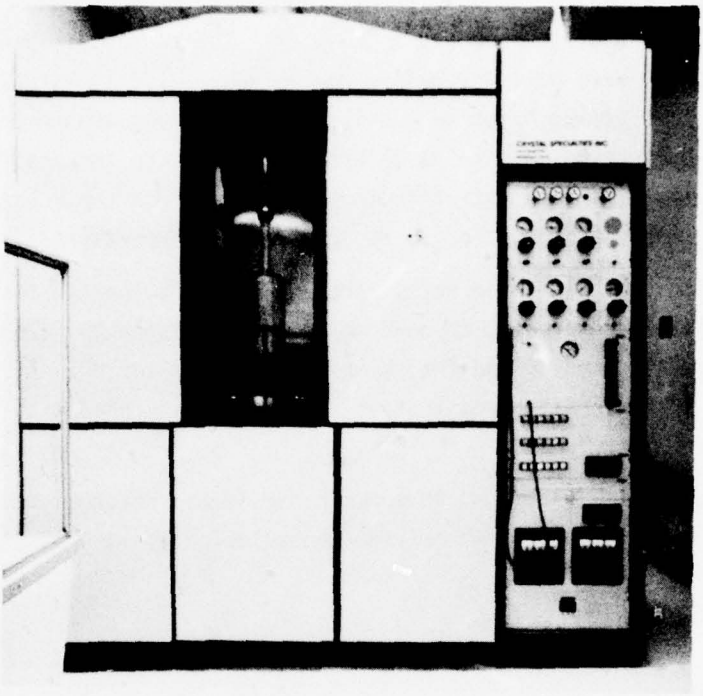


Figure 4-1. Epitaxial Deposition Reactor

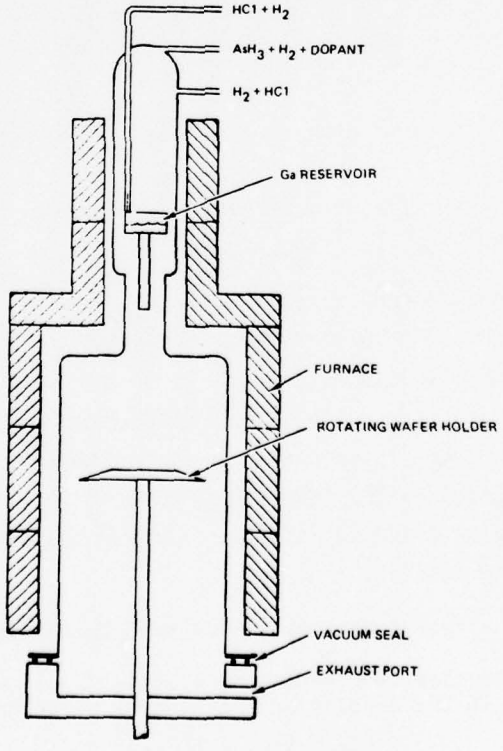


Figure 4-2. Schematic of EPI Reactor

The resistance heated furnace is split and operates in a "clam shell" motion which aids in rapid cooling of the deposition chamber. The furnace is equipped with heat shields which cover each half of the furance. These serve to establish an equilibrium temperature in the furnace prior to locking the two halves around the reactor tube, permitting the deposition chamber to be brought rapidly to the desired deposition temperature. This minimizes out-diffusion of dopants from the substrate during the time the wafer is being brought up to the deposition temperature.

The reaction tube has three entry ports for introducing the reaction gases. One port contains the Ga reservoir, through which HCl is passed to form GaCL. Another port is used for AsH_3 and H_2 and the third port is used for HCl and H_2 for etching and control of the free carrier concentration. The layer is doped with H_2S which is introduced in the AsH_3 port.

The gallium, which is heated in a reservoir in the reaction tube, is delivered to the depostion zone in the form of gallium monochloride by the reaction of HCl with Ga as

$$Ga_{(s)} + HCl_{(g)} \rightarrow GaCl_{(g)} + 1/2\ H_{2(g)}$$

GaAs is formed as the reaction proceeds with the introduction of arsine from a source cylinder of 10% arsine in hydrogen

$$AsH_3 \rightarrow 1/4\ As_{4(g)} + 3/2\ H_2$$

$$1/4\ As_4 + GaCl_{(g)} + 1/2\ H_2 \rightarrow GaAs + HCl$$

The epitaxial layer growth rate is determined by the mole fraction of the reactants in the vapor phase and the substrate temperature.

The mole fractions are controlled by the flow rate of the arsine and the flow rate of HCl over the gallium. The gallium temperature and the HCl flow rate over the gallium reservoir are controlled such that nearly 100 percent of the HCl is converted to the gallium monochloride. Variation in the growth rate may cause both the free carrier concentration and the layer stoichiometry to vary. Under optimum conditions the growth rate is varied by dilution rather than via changes in the mole fraction. Mole fraction changes are less repeatable and may tend to increase the compensation factor as indicated by decreases in the mobility.

High resistance buffer layers may be achieved by one of the following means:

- Controlling undesired doping species, such as silicon, by preventing its formation in the deposition reaction by using an excess of HCl

$$4\ HCl + SiO_2 \rightarrow SiCl_4 + H_2O$$

- Controlling the stoichiometry of the reaction – excess gallium tends to make the layers P-type while excess arsine makes the wafer N-type. This type of control, by compensating, may cause the mobility to be lower than in the case when HCl is used to prevent the Si species from forming

- Intentional doping with a foreign atom such as Cr, O, or Fe.

TRW has placed emphasis on the first two techniques, with the excess HCl process being the most successful.

Epitaxially deposited layers may be intentionally doped to a range up to 5 x $10^{18} cm^{-3}$ using sulfur from a 10% H_2S source in hydrogen as a carrier gas. This technique starts by first achieving a buffer quality condition in the reactor and subsequently doping to the desired level.

The morphology of the deposit depends mainly on the preparation of the substrate surface prior to deposition and on the stoichiometry of the deposit. It is quite easy to obtain deposits with a low density of defects if the layers are stoichiometric and deposited at high temperatures. High purity layers generally are deposted at lower temperatures and with a Ga rich mixture. As the gas phase composition is changed towards an arsenic-gallium ratio of 1:1, the growing deposit becomes more sensitive to the presence of particulate matter and defects such as scratches produced by wafer preparation and handling. In some cases substrates, which showed no surface features when examined with an optical microscope, have given high purity buffers, but with excessive scratches whose presence was revealed only after the depositions.

With low HCl concentration, buffer layers are obtained when the ratio of arsenic atoms to gallium atoms lies within a narrow range. At the gallium-rich end of this range, a pit-like defect becomes prominent. This defect gives a hazy appearance to the deposit. It is probably caused by the byproduct hydrogen chloride in the GaAs synthesis reaction shown above, or, in a different form, in the following reaction

$$GaCl_{(g)} + 1/2\ H_{2(g)} \rightarrow \left(Ga_{(s)} + HCl_{(g)}\right)$$

Haze is also produced by the evaporation of arsenic from the substrate during the heatup prior to deposition. This type of haze is caused by thermally produced pits and is eliminated by allowing the arsine to flow during the heatup cycle.

The epi wafers deposited during this program phase were used to develop the planar TED process. The doping concentration of the epi wafers was 3 x 10^{16} with a thickness of 0.8 μm. The doping concentration was achieved with a ±10% accuracy. The epitaxial layer thickness may also vary ±10% across the wafer but can be anodically trimmed to within ±3% of the desired value. A typical distribution of peak currents of TED pairs made on a wafer is shown in Figure 4-3. The calculated sheet resistance is recorded on the chart below the peak current values. This wafer was not thinned by anodization.

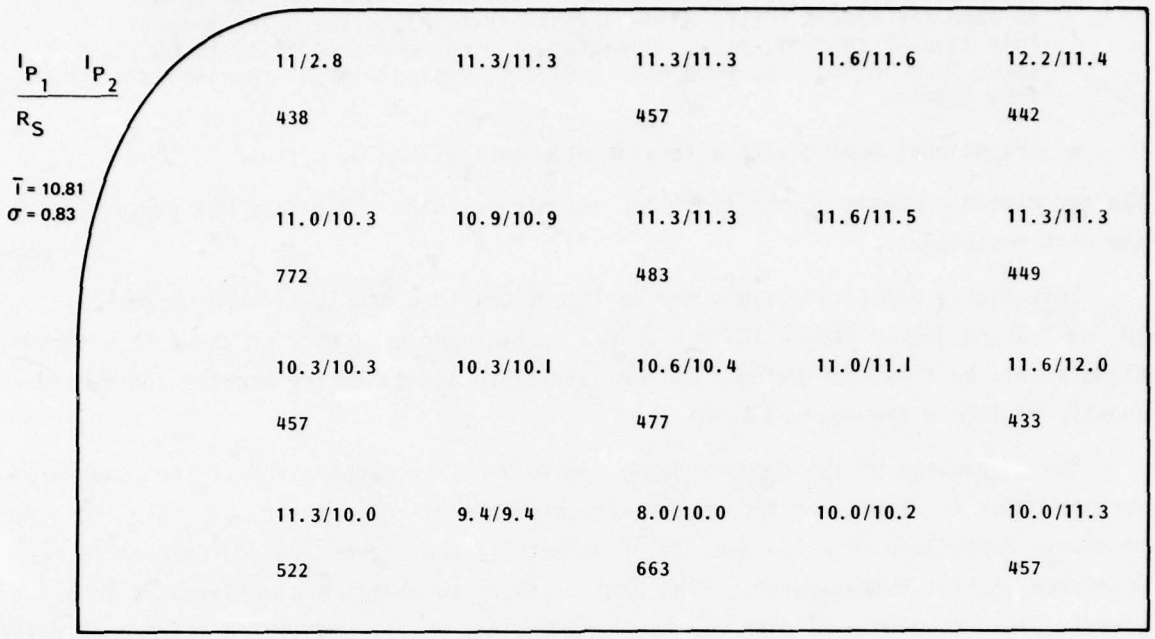


Figure 4-3. Distribution of Peak Current and Sheet Resistance across a Mesa TED Wafer

A tighter distribution is possible with anodization trimming (discussed in Section 4.2).

4.1.2 Ion Implantation Technology

Ion implantation into GaAs in a predictable manner was a major goal in the first phase of this development program. The repeatability of the desired doping profiles is dependent upon many factors; these include the various collision processes in implanting the ion, the substrate quality of the ionic species, the lattice defect structure, and the post implant treatment.

Ion implantation provides a means for introducing precise amounts of impurity elements with controlled doping profiles into semiconductor materials. The depth or range of the implants is determined by the ion energy and various loss mechanisms. As the ion enters the solid target or substrate, it loses energy and comes to rest by interacting with electrons in the target and by collision with the target nuclei. To a first approximation, the distribution is determined in a predictable manner from the ion energy and mass of the target atoms. In an amorphous target, the distribution of the implanted species is nearly gaussian and may be described by a projected range R_p and standard deviation ΔR_p as

$$N(X) = \frac{D}{(2\pi)^{2/3}\,\Delta R_p} \exp\left[-(X-R_p)^2/2\Delta R_p{}^2\right]$$

where X is the perpendicular distance into the substrate and D is the ion dose. Both R_p and ΔR_p can be calculated according to LSS theory.

In crystalline targets, the distribution depends on orientation. If the ions are implanted parallel to a major axis or plane, some of the ions can penetrate to depths much deeper than predicted for amorphous targets. The effect is called cahnneling. To achieve predictable and reproducible ion implanted profiles in the crystal, methods to prevent channeling must be employed. These include orienting the target with respect to the ion beam in a nonchanneling direction or using an amorphous layer over the crystalline target during implantation.

To achieve the desired doping profile by ion implantation, several factors had to be considered. These included the doping species, the implant conditions, the post implant anneal, and the annealing cap.

The doping species which have been investigated during this program are listed in Table 4-1. The range of Se is about one-half that of Si and S at the same implant energy and the diffusion coefficient is less; therefore, one anticipates a more abrupt profile of concentration vs depth for Se than for S or Si. It has been observed that S implants into GaAs show a large deviation from the gaussian profile, and the R_p and ΔR_p do not adhere to the LSS theory.

Table 4-1. LSS Range and Standard Deviation of S, Se, and Si Ions in GaAs

Species	Energy keV	Range R_p (μm)	Standard Deviation (μm)
S	100	0.0740	0.0387
	200	0.1509	0.0667
Se	200	0.0695	0.0313
	400	0.1371	0.0557
Si	100	0.0850	0.0442
	200	0.1739	0.0753

Experimentally, Se and Si are both found to be well behaved relative to LSS theory; however, experience indicates that Se must be implanted into a heated substrate to minimize collision damage.

As ions are implanted into a substrate, the collisions with the lattice atoms transfer sufficient energy to displace atoms from the lattice causing vacancies and interstitials and sometimes long range disorder in the crystal. The amount of disorder is dependent on the ion species, the temperature of the substrate during implant, and the dose.

The lattice location of implanted species is dependent on a number of complex reactions. These can be classified as: substitutional reactions, interstitial reactions, and irregular reactions.

Experiments suggest[1] that the major native defects in GaAs are of the form

$$V_{As}^{X},\ V_{Ga}^{X},\ (V_{Ga})_2^{X}$$

and appropriately charged versions characterized by the following reactions

$$0 \rightleftarrows e^{-} + h^{+}$$

$$0 \rightleftarrows V_{Ga}^{X} + V_{As}^{X}$$

$$2\ V_{Ga}^{X} \rightleftarrows (V_{Ga})_2^{X}$$

$$V_{Ga}^{X} \rightleftarrows V_{Ga}^{-} + h^{+}$$

$$(V_{Ga})_2^{X} \rightleftarrows (V_{Ga})_2^{-} + h^{+}$$

Defects introduced during implantation are removed by appropriate thermal treatments, which are performed during the implantation as well as by post-implantation annealing. Since GaAs tends to dissociate during high temperature annealing, this dissociation must be minimized by capping the implanted sample prior to annealing. Capping materials act as a mask against the out-diffusion of the constituents of the compound semiconductor and the implanted species. The choice of annealing cap will be discussed later.

In the case of N-type dopants in GaAs, a one-to-one relation between implanted dopant atoms and resulting active carriers has generally not been observed. Doping efficiency, which is defined as the ratio fo the number of active carriers introduced in the GaAs to the total number of implanted dopant atoms, is related to several factors. Dopant atoms can occupy the wrong site in the crystal lattice, and redistribution of the background Cr-dopant in the semi-insulating material may occur. Diffusion of the implanted dopants may take place, resulting in a doping profile which is substantially different from the expected range profile of the implanted dopants. Diffusion of defects may also occur which causes nonstoichiometry and may have adverse effects on the electrical activity resulting from the implantation. It has been suggested, for example, that while implanting an N-type dopant in GaAs of the kind which should occupy arsenic sites, an equal amount of gallium should also be implanted.[2]

Channeling effect studies[3] indicate that appreciable annealing occurs with low dose implants when the substrate is heated to 200°-400°C during ion implantation. This annealing is incomplete, especially for high dose implants. Post implant annealing at higher anneal temperatures is usually required. With high dose implants, some residual implant damage has been observed even after annealing at temperatures as high as 900°C.

The optimum annealing temperature is determined experimentally as the lowest temperature at which a practical doping efficiency can be achieved without excessive diffusion of the implanted ion. High temperature annealing of GaAs above 600°C results in appreciable dissociation. To prevent this dissociation, a number of annealing techniques have been used. These include adjusting the ambient such that the partial pressures of the components of the GaAs do not exceed that of the ambient and the use of various encapsulants. These techniques are discussed in Section 4.2.4.

4.1.3 Processing Technologies

Other standard processing technologies used in fabricating the experimental devices include photolithography and oxidations, and metallizations for the ohmic contacts, Schottky gates, and for interconnections between the various devices. A positive photoresist was employed throughout the program for better line definition of the small geometry devices. These resist materials were used with the "lift" technique and in conventional etching processes, such as mesa etch and interconnect metal pattern definition.

Low temperature (390°C) deposited SiO_2 films are used in our process for the dielectric isolation. We have also investigated sputtered oxides but the deposition rates were too slow for this application.

The standard ohmic contact is formed from an evaporated AuGe alloy, although both evaporated and sputtered contacts have been studied. A photoresist film is used to pattern the ohmic contact. Approximately 1000 Å of AuGe followed by a Pt layer is deposited on the wafer. The Pt acts as a barrier between the Au and the interconnect metal. It also helps to prevent balling of the ohmic contact during subsequent alloying at 450-500°C. Following evaporation, the background metal and photoresist are lifted in suitable solvents.

Aluminum gates have been employed throughout the technology development because they are stable up to 500°C and compatible with the oxides used as the dielectric material in the capacitors and undercrossings. Other gate metals have been investigated; e.g., TiPtAu and TiWAu. These are more difficult to process, but offer some advantages over the aluminum gates.

The interconnect metal used in the standard process is sputtered Ti-Al. This has been successful in simple circuit fabrication but is one of the areas requiring additional study.

4.2 PROCESS DEVELOPMENT FOR ANALOG CIRCUITS

The process development described in this section reflects the process improvements and the technology developments which were necessary to meet the program objectives. Improvements in the ion implant uniformity and repeatability were direct results of substantial improvements in the post implant capping, anneal technique, and substrate selection procedure.

The process developed for planar TEDs employed a boron isolation implant and good control of the epi material. The epitaxial material control was improved with the implementation of the anodization thinning technique. This development has yielded improvements in the device technology and has been demonstrated on discrete and monolithic circuit test vehicles. These procedures are described below.

4.2.1 Gallium Arsenide Substrate

The objective of the material investigation was to provide suitable substrates for establishing a repeatable ion implant and epitaxy process. Substrates were evaluated from seven suppliers with only a few crystals qualified for epi and ion implant processing.

The substrates used in this program are Cr doped semi-insulating material grown on the (100) orientation. Wafers purchased for epitaxial processing are cut 3° off the (100) orientation toward the (110) direction.

The Cr doped substrates were purchased to the following specification:

- Dislocation density: $<10^3 cm^{-3}$
- Resistivity: $>10^7$ Ω/□
- Crystal growth along the 100 direction to permit growth of square crystals
- Finished wafer thickness: 16 mils thick
- Must pass thermal conversion test.

Some suppliers will guarantee wafers to withstand certain temperatures without conversion, while others will provide sample wafers for characterization before the entire crystal is purchased. The conversion test has been employed to evaluate wafers for ion implant applications and for epitaxial processing. Some wafers have been found to be suitable for epitaxy processing but unsuitable for ion implantation. These are wafers which do not convert with thermal testing but convert after ion implant.

The thermal conversion test is performed by capping the substrate with a suitable capping material and heating at 850°C in H_2 for 30 minutes. The cap is removed and conductance test performed. Wafers which show surface conduction at this point are considered poor quality for either epitaxial depostion or for ion implantation.

Wafers that pass this test may be suitable epitaxy processing but yet unsuitable for ion implantation. These wafers are given a second test to determine if damage enhanced diffusion will cause the wafers to convert during the implant anneal. This may be evaluated either by using a nonreactive[4] species such as Ar or Kr to implant before performing the conversion test or by using a calibration implant schedule to determine conversion.

The calibrated implant schedule used by TRW is 100 keV Si+ at a dose of $3 \times 10^{12} cm^{-2}$. This schedule, when used with qualified substrates, gives very steep carrier concentration vs depth profiles. Typical profiles of good and poor substrates are shown in Figure 4-4. The characterization data of wafers from various suppliers is given in Table 4-2.

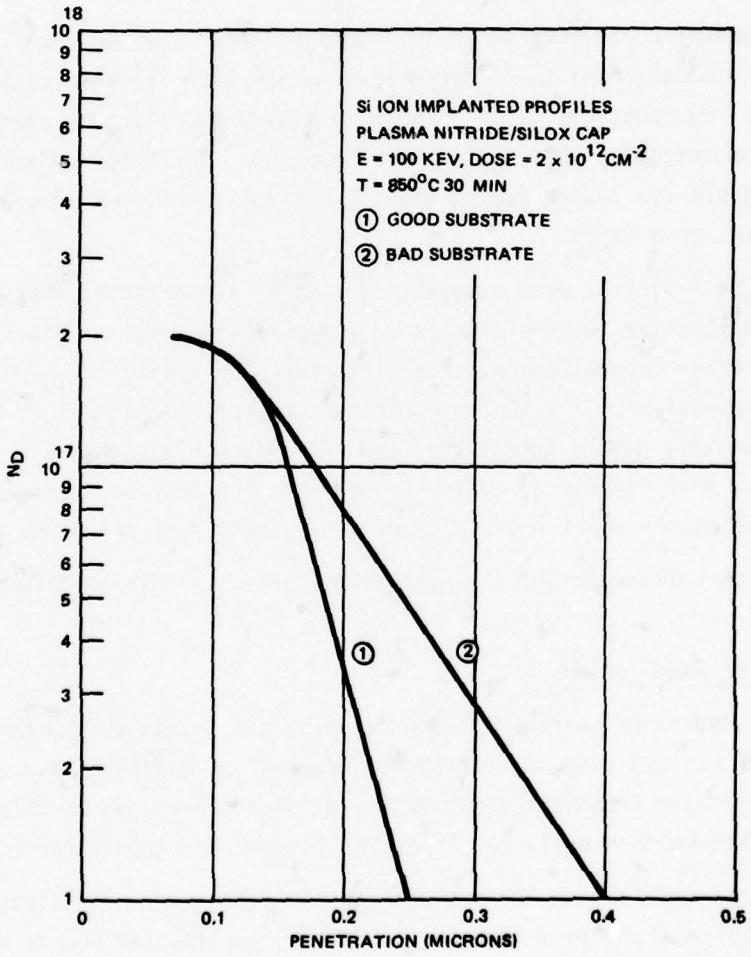


Figure 4-4. Concentration versus Depth Profile for Good and Poor Substrates

Table 4-2. Material Evaluation Summary

Vendor	Crystals	Good
A	6	2
B	1	0
C	1	0
D	2	0
E	1	Inconclusive
F	1	0
G	1	-

Criteria: 1) Thermal conversion with a cap

2) Implant profile after 100 keV Si implant of $3 \times 10^{12} cm^{-2}$ exhibits uniform peak concentration with minimum "tailing"

A good ion implant profile is shown in Figure 4-5 for ingot No. 8. The peak concentration for diodes across the wafer does not vary over 15% and the implant's tail is not broad. By contrast, ingot 9 shown in Figure 4-6 has a broader implant tail and a peak concentration that varies more than 20%. While the wafers from both crystals may be usable for device fabrication, ingot 8 is preferred when one is trying to match devices on a wafer.

Ingot 7 (Figure 4-7) is a more exaggerated case of a nonreproducible peak N with broad diffusion tails after ion implantation. A profile from this ingot is also depicted in Figure 4-8 after thermal anneal only. It gives the appearance of having an ion implant to a concentration of 2×10^{16} even though no implant was made. The crystal shows thermal conversion at the anneal step and normally would have been rejected without the ion implant test results given in Figure 4-8. The test for conversion is also performed by measuring the sheet resistance of the wafer before and after thermal anneal.

The data for specific wafer lots qualified and processed during this program are shown in Appendix C.

4.2.2 Self-Limiting Anodization

The necessary degree of control of both impurity concentration and thickness of the epitaxial layer has not been satisfactorily achieved by epitaxial deposition. A self-limiting anodization technique after epitaxial growth provides an alternative which produces a more uniform epitaxial layer for integrated circuit fabrication.[5]

Essentially, the anodization is an electrochemical process. The electrolyte and the epi layer interface resemble a Schottky junction. Anodization occurs when the bias applied at the interface creates avalanche breakdown in the GaAs. Gallium ions move out to the interface, react with the oxygen ions, and a layer of oxide is formed

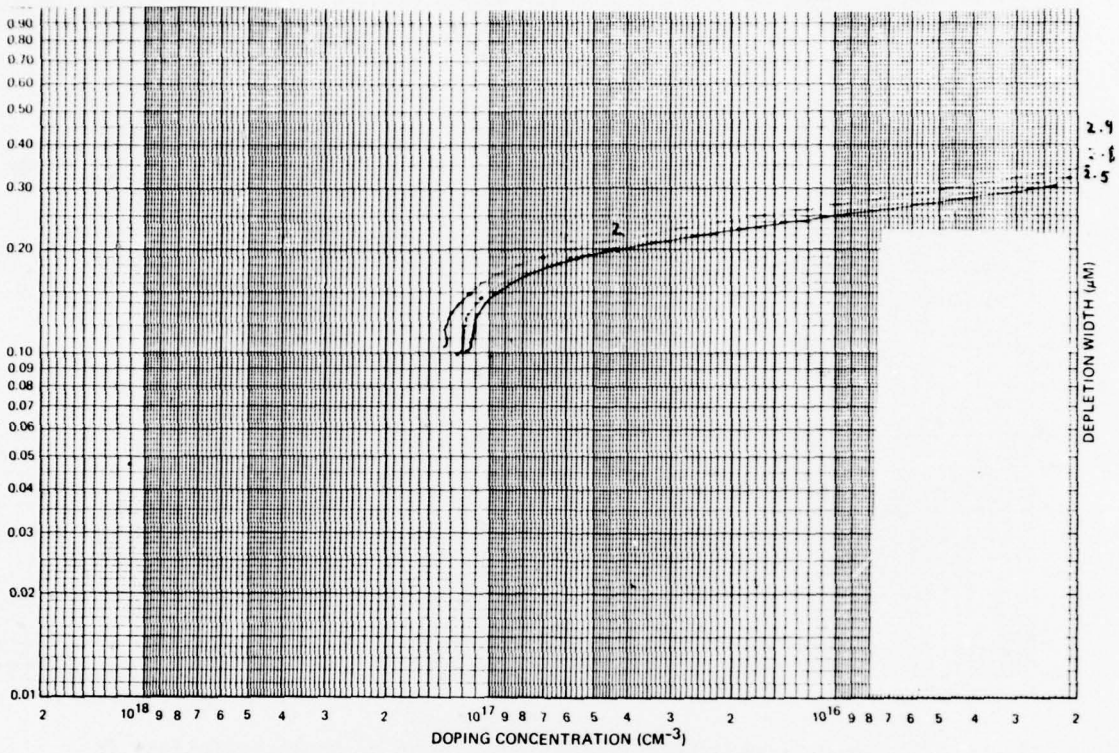


Figure 4-5. Profile of Test Implant into Wafer from Ingot #8. Substrate Shows Repeatability Characteristics and Sharp Slope in Implant Tail

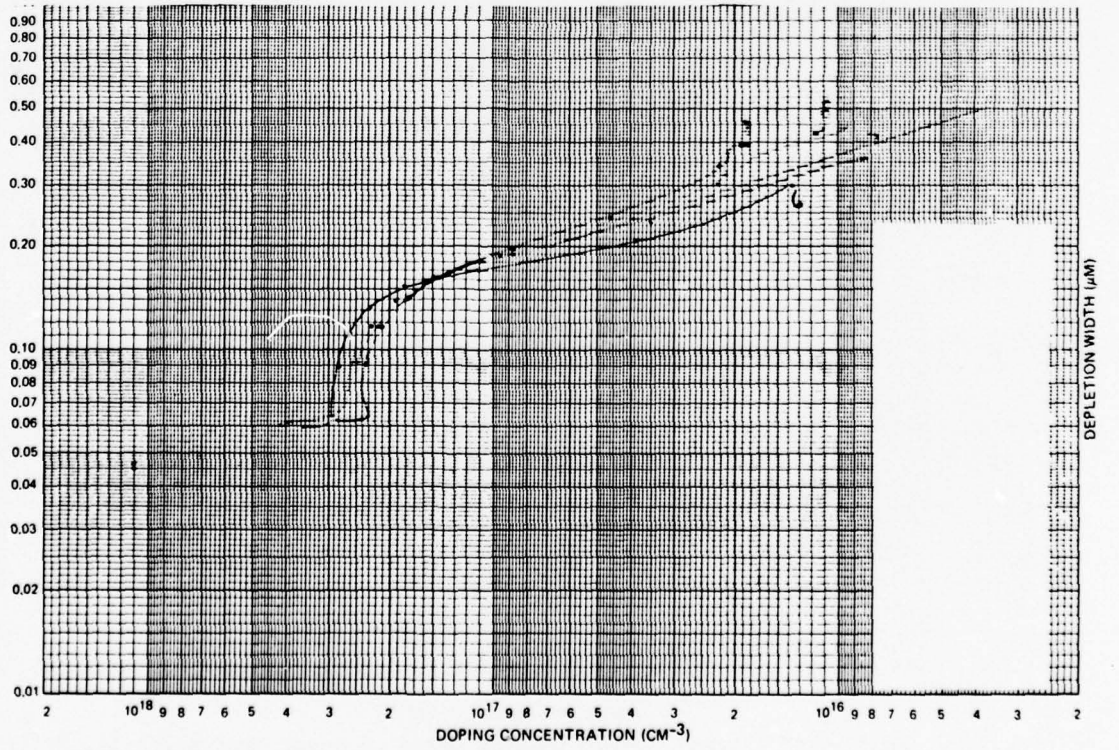


Figure 4-6. Profile from Test Implant into Wafer from Ingot #9 Shows Nonreproducible Profiles

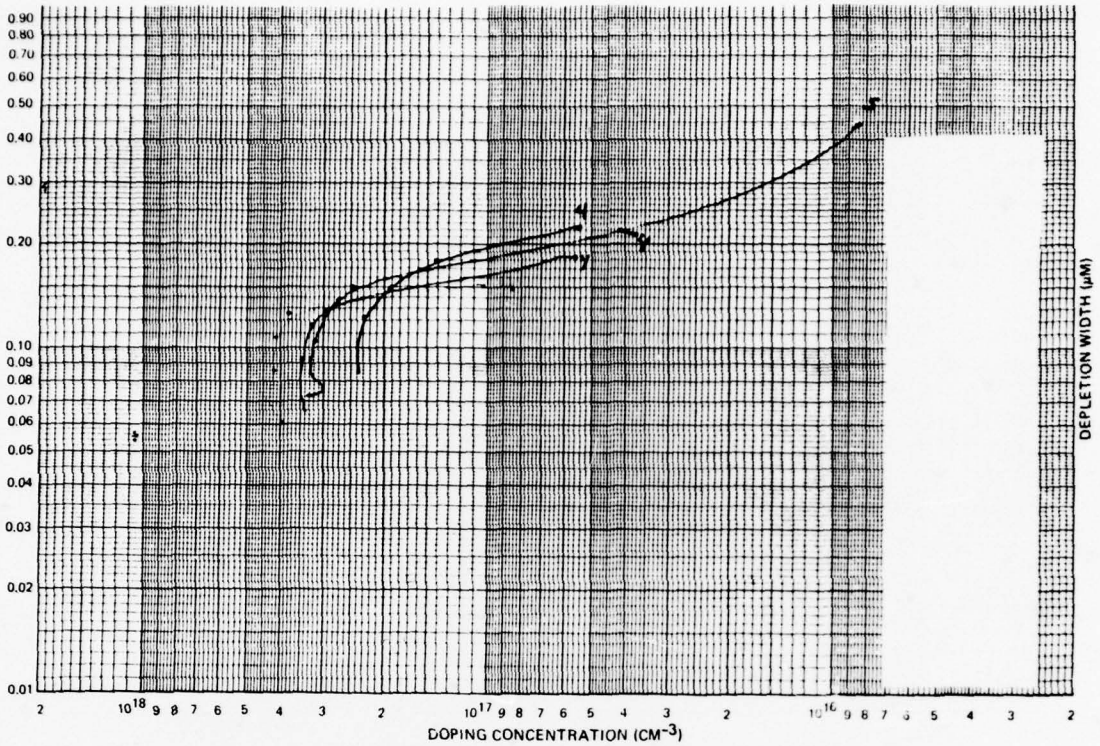


Figure 4-7. Profile from Test Implant into Ingot #7 Shows Variations in Peak Concentration and Broad Characteristics in the Tail Region

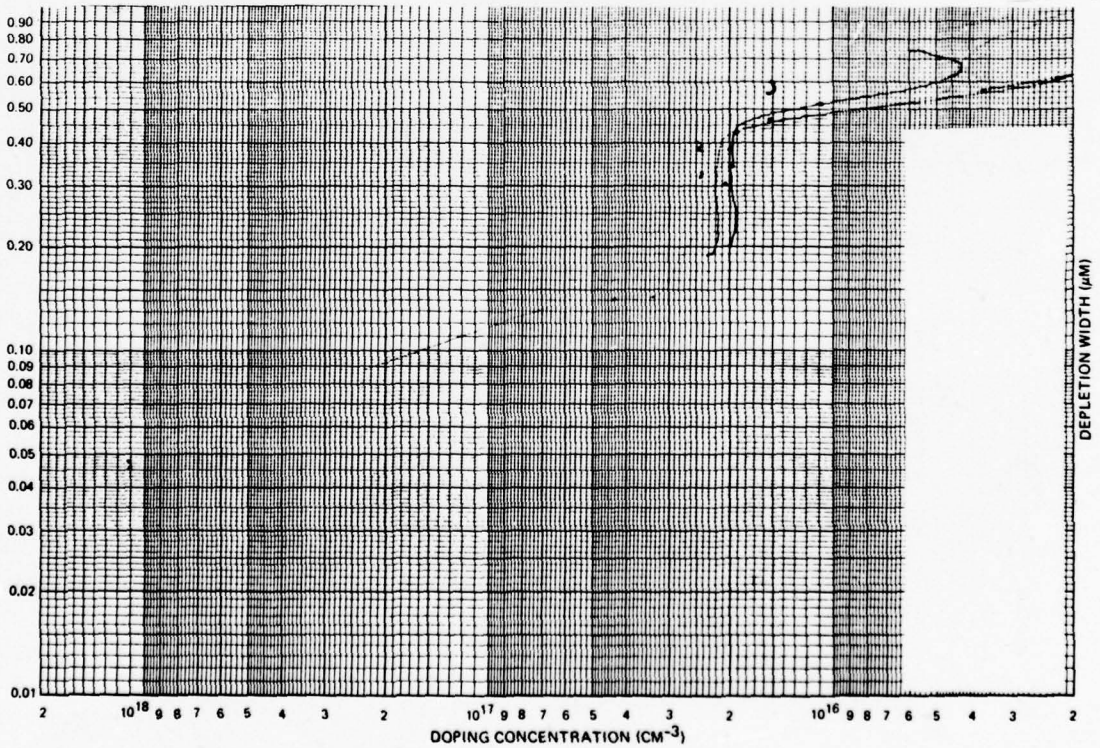


Figure 4-8. Profile of Thermal Conversion Test made on Wafer from Ingot #7, Prior to Test Implant. Shows a background concentration of $2 \times 10^{16} cm^{-3}$ at about 0.4 microns from the surface of the wafer.

at the interface. As the oxide thickness increases, the surface potential at the gallium arsenide surface decreases. Once the surface potential drops below the breakdown voltage the anodization stops.

Figure 4-9 depicts the impurity concentration, electric field, and voltage distributions in the gallium arsenide. When the anodization first starts at the surface, the surface electric field equals the fields required for avalanche breakdown, E_m. As the anodization continues, the zero field point moves further into the active layer. When this point reaches the active and buffer layer interface, the voltage drop occurs in the buffer layer. Since the buffer layer has a lower impurity concentration, the slope of the electric field is much less than that in the active layer. Consequently the surface potential drops. The surface electric field will drop to a value less than E_m and anodization stops. The final active layer thickness ℓ can be predicted by approximating the electrolyte-gallium arsenide interface as a one side abrupt junction

$$\ell = \overline{W}_m = \sqrt{\frac{2\varepsilon_s \overline{V}_m}{qN_d}}$$

where $\overline{V}_m$ is the breakdown voltage and W_m is the maximum depletion width. If there is a slope in the concentration distribution at the active and buffer layer interface, the final active layer thickness ℓ becomes

$$\ell = \sqrt{\frac{2\varepsilon_s \overline{V}_m}{qN_d}} - \alpha$$

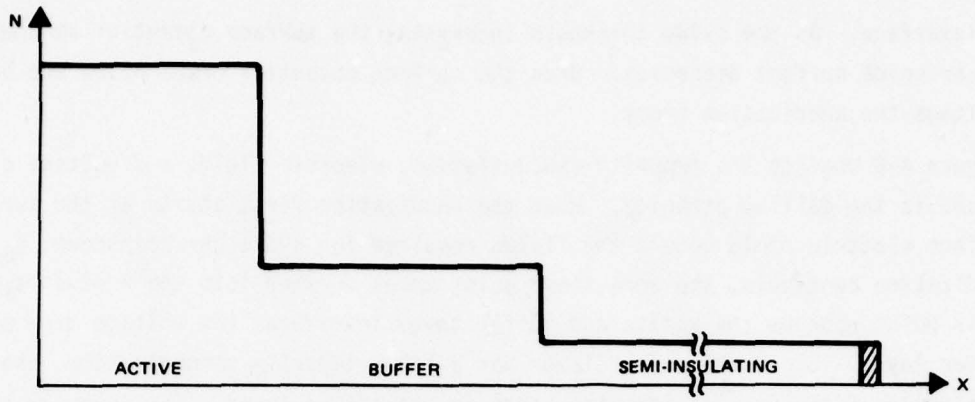
where α is the distance for a decade change of impurity concentration.

After a uniform thickness is reached, light is used to stimulate further anodization to the desired thickness. The setup for anodization is shown in Figure 4-10. The electrolyte is 3% aqueous solution of tartaric acid mixed with two volumes of propylene glycol. The pH value of the solution is adjusted to 6.2 with NH_4OH. The gallium arsenide substrate is mounted on an epoxy laminar board with a copper contact imbedded in the board. A platinum electrode is used as the cathode. With this self-limiting process, we are able to control the Nd product to within $\pm$3% variation for a wafer of 1.0 square inch. The Nd plot of a typical wafer is shown in Figure 4-11.

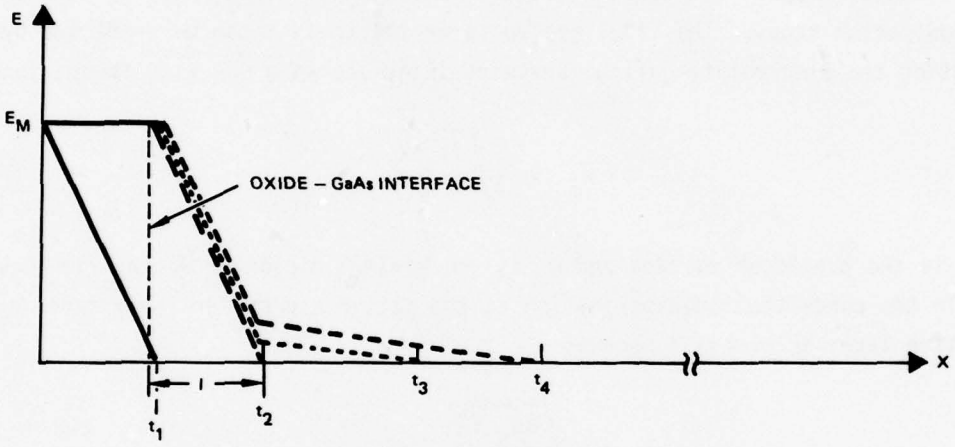
4.2.3 Ion Implantation Development

Several major milestones were achieved in the ion implantation technology development. These included:

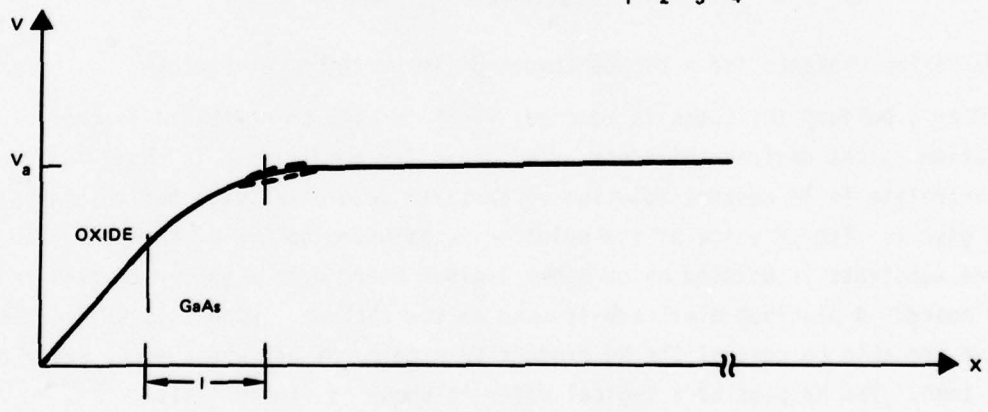
- The development of a predictable ion implant profile
- The development of an N+ ion implant procedure



(a) IMPURITY CONCENTRATION DISTRIBUTION



(b) ELECTRICAL FIELD DISTRIBUTION AT $t_1 < t_2 < t_3 < t_4$



(c) VOLTAGE DISTRIBUTION

Figure 4-9. Concentration Field and Voltage Profiles

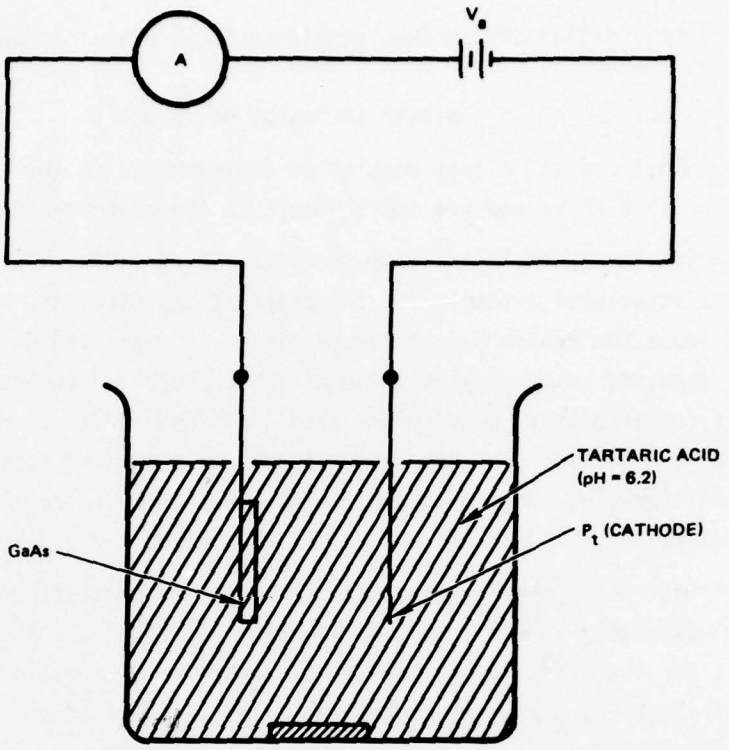


Figure 4-10. Anodization Setup

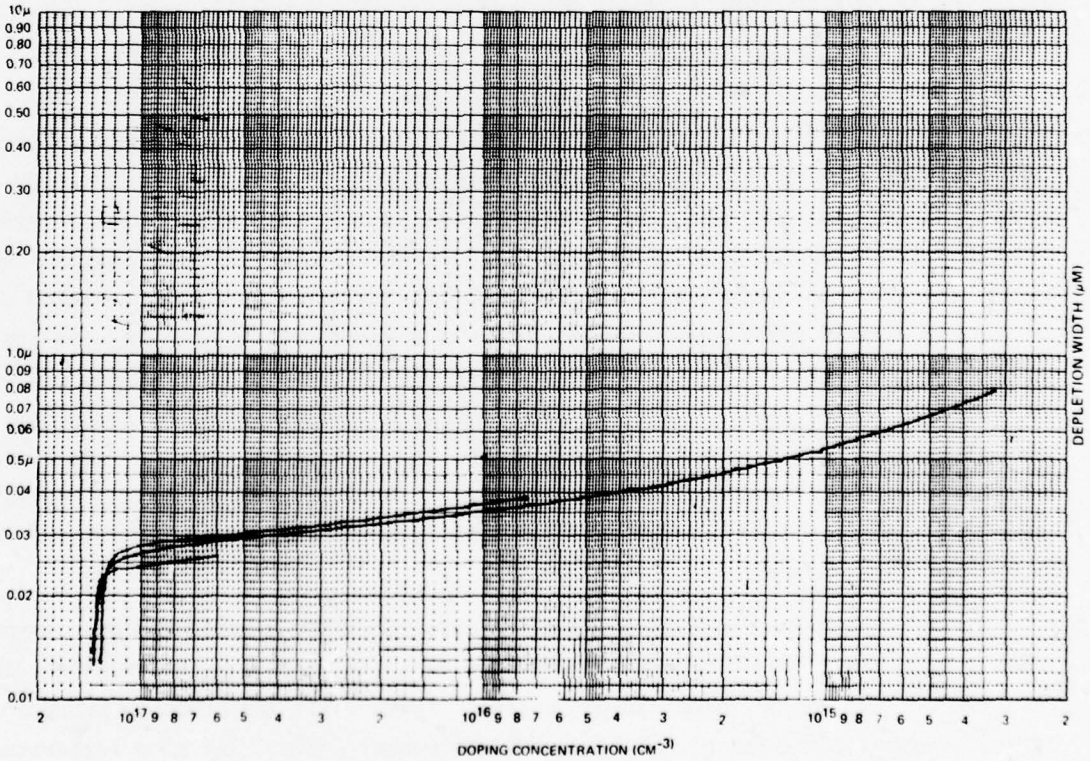


Figure 4-11. Concentration Versus Depth for Thinned Epilayer

- The demonstration of masking techniques for a planar (channel implant) process
- The establishment of a planar (B isolation) process.

These achievements are the direct results of improvements in the material selection technique described above and the improvements in the capping and annealing techniques.

The ion implant technologies were directed toward device improvement and fabricating device structures suitable for the proposed LSI circuits. The test circuits require ion implanted active layers formed either in qualified Cr doped substrates or epitaxially deposted buffer layers. The ultimate choice of targets will be made on the basis of repeatability, performance, and qualified substrate availability. Presently there is a bank of over 200 square inches of qualified substrates for ion implant. Additionally, the proposed circuits can be fabricated in either buffers or Cr-doped substrates.

For the test vehicle being studied, the doping concentration in the implanted layer is approximately $10^{17}cm^{-3}$ at a depth of 0.1 μm to give a pinchoff voltage of about 1 volt for the FETs. Additionally, N+ layers were investigated in the ohmic contact region where a doping concentration of about $4 \times 10^{18}cm^{-3}$ for improved contact resistance was achieved. Both of these active layers were achieved with Si+ implants. The process employed in achieving repeatable implants and the processing results are discussed in this section.

The N-type implant dopants investigated at TRW include S, Se, and Si ions. Very high purity beams have been obtained with all three ion species: S^{+}_{32}, Se^{+}_{79} and Si^{+}_{28}. The fluorides of these dopants have been used as source material and most of the implants were carried out using a cold cathode source. The ions were implanted into both Cr-doped substrates and semi-insulating epitaxially deposited buffer layers. The substrate material is grown on the (100) orientation, while the epitaxial buffer layers are grown on substrates 3° off of the (100) orientation. The implanted wafers are capped with RF plasma-deposited Si_3N_4 films covered with SiO_2. They are annealed at 850°C for 30 minutes in a N_2 flowing atmosphere and 900°C for ion doses greater than $10^{13}cm^{-2}$. The profiles are measured both by capacitance voltage techniques on specially fabricated Al Schottky diodes and by the conventional Hall effect method. In some cases, a differential Hall measurement using anodic stripping techniques is used as a cross-check of the C-V profiles. Electron mobilities are calculated from the Hall effect measurements.

Figure 4-12 shows two typical profiles obtained after S implantation. Both profiles show a considerable broadening compared to the theoretical LSS profiles, thus resulting in much deeper penetration "tails." These tails are probably produced by defect enhanced diffusion of S ions during the anneal cycle. The room temperature

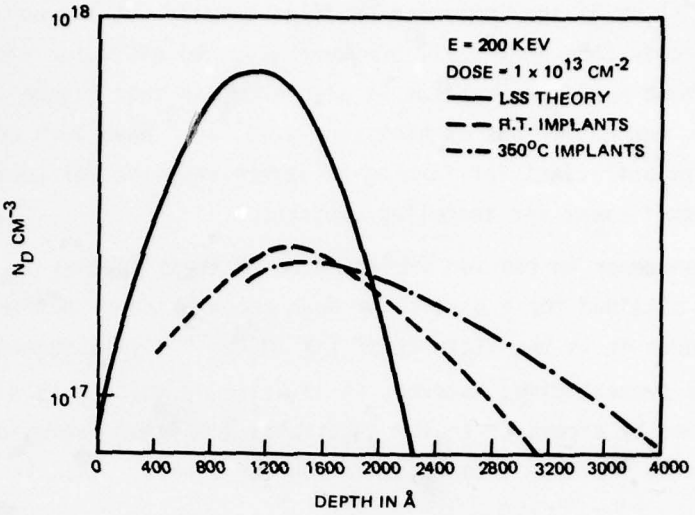


Figure 4-12. S-Implantation Typical Profiles

implanted profile shows somewhat less broadening than the hot implant. It is noteworthy that S behaves in a very anomalous way in GaAs since the peak electron concentration ($N_D$max) obtained after ion implantation is always in the vicinity of $2 \times 10^{17} cm^{-3}$ independent of the ion implantation dose. Consequently, S implantation is viewed as not very useful for GaAs integrated circuits.

Figure 4-13 shows a typical Se ion implanted profile carried out at 350°C. This profile shows considerable improvement as compared to the S implants.

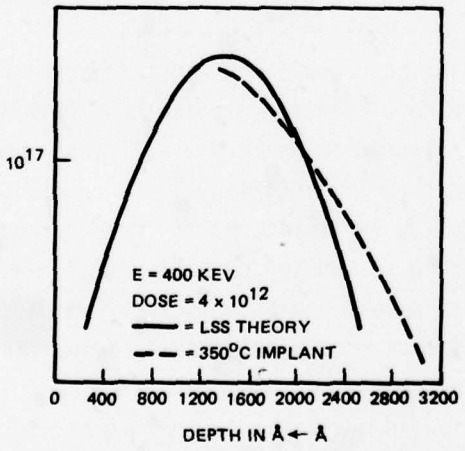


Figure 4-13. Typical Se Ion Implantation Profile

Figure 4-14 shows Si ion implanted profiles carried out at room temperature. The low dose implants show very small broadening due to diffusion effects. The profile obtained from a high dose implant is also shown in this figure ($\approx 10^{14}$ cm^{-2}). As the figure shows, concentrations as high as $4 \times 10^{18} cm^{-3}$ have been obtained. These concentrations are sufficient for forming N+ layers required for good ohmic contacts but perhaps not sufficient for tunneling contacts.

A common phenomenon in the ion implantation of these species is that a certain minimum $N_D max$ is obtained for a particular dose below which no active layer can be detected. This dose is in the vicinity of $1 \times 10^{12} cm^{-2}$. This phenomenon is not clearly understood at the present time; however, it is believed that it is due to a high trap density caused by excess Cr in the substrates. A lower doping concentration can be achieved with implants into epitaxial buffer layers. This is currently being investigated.

A large number of discrete FETs and integrated circuits using this implant process have been processed. Ion implanted FET devices fabricated at TRW are compared in Table 4-3, and discussed in detail in Section 4.4.

Table 4-3. Results of S, Se, and Si Ion Implantation into GaAs

Species	Energy keV	Dose cm^{-2}	Implant Temp °C	Doping Efficiency %	N_D Max cm^{-3}	FET V_p Volts
S	150	1×10^{13}	350	25-50	2×10^{17}	3-5
Se	400	4×10^{12}	350	80	2×10^{17}	2-3
Si	100	3×10^{12}	RT	80-90	1.5×10^{17}	1-2

A number of studies have been published about Si ion implantation into GaAs. These reports cover carrier concentration profile and mobility distributions,[6] the effects of dose rate and implantation temperature,[7] and the difference between room temperature and high temperature implantation.[8] A comparison has been made between Si and other donor impurity ion implantation.[9] More recently, depth distribution profiles of Si implanted at 50 to 500 keV have been measured by secondary ion mass spectrometry. These studies report doping efficiency values lower than 50% for low dose implants ($\leq 10^{13} cm^{-2}$) except when pyrolytically deposited Si_3N_4 is used as an encapsulant when 70% was obtained.[10] No information on uniformity and reproducibility of Si ion implantation is available in the literature. The published data suggests that all of the experiments were carried out on a small scale.

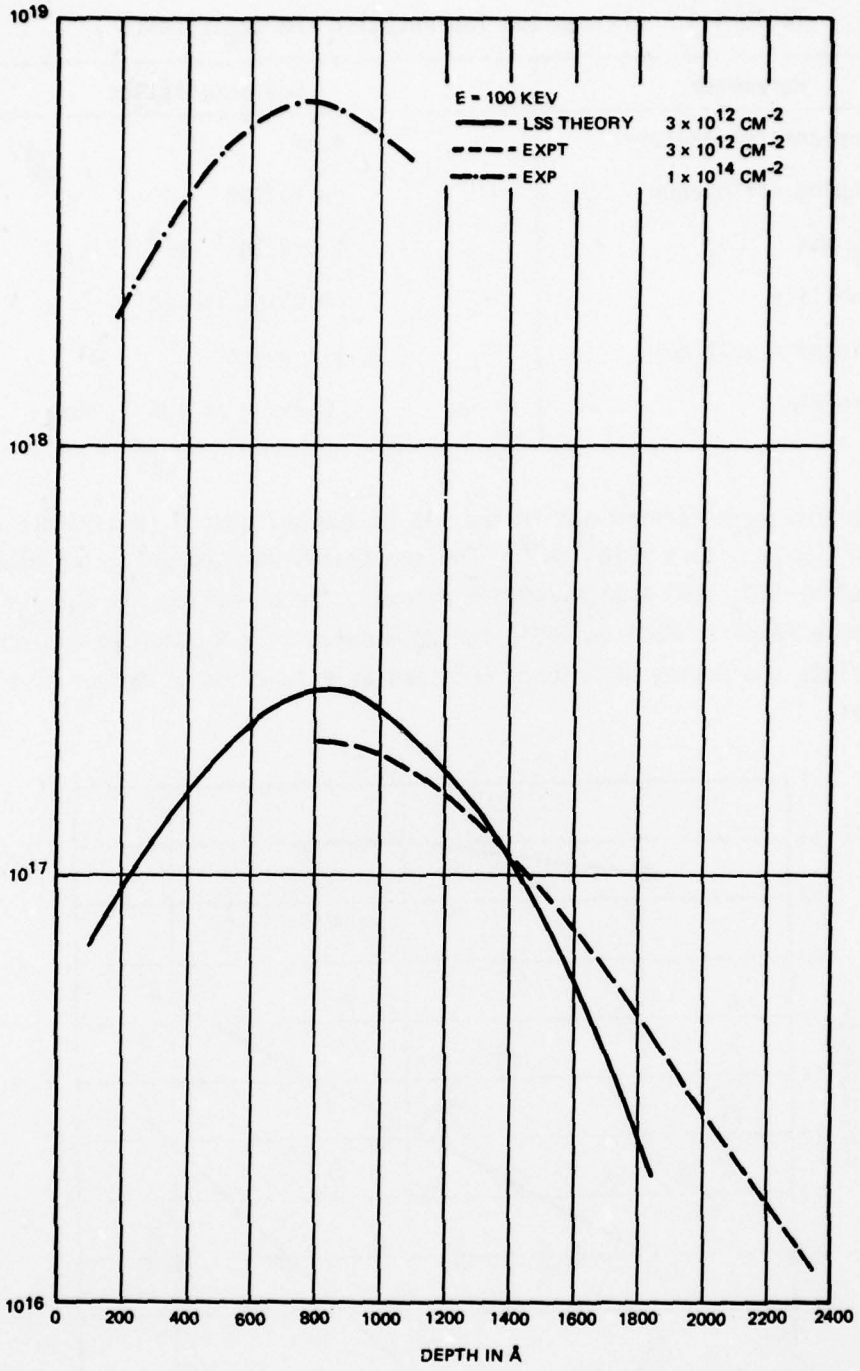


Figure 4-14. Si Ion Implantation at Room Temperature

TRW has conducted extensive development on this program using Si ion implantation. As a result of this development a reproducible process for ion implant into substrates has been established. The characteristics of a typical implant are shown in Table 4-4.

Table 4-4. Silicon Ion Implantation Characteristics

Parameter	Characteristics
Inplant temperature	Room
Doping efficiency	Up to 90%
N_D max	1.5×10^{17} cm^{-3}
Mobility	>4500 cm^2/V-sec
Pinchoff voltage	1-2 volts
Profile	<0.15 μm at 10% N_D max

Ion implants were carried out in the 100 to 200 keV energy range and a dose ranging from 1×10^{12} to $1 \times 10^{14} cm^{-2}$. The substrates were capped using plasma Si_3N_4 films covered by SiO_2 (900 Å Si_3N_4/4000 Å silox). The annealing was carried out in the temperature range of 800° to 900°C for 30 minutes in a N_2 flowing ambient. Figure 4-15 depicts the doping efficiency obtained as a function of temperature for several doses.

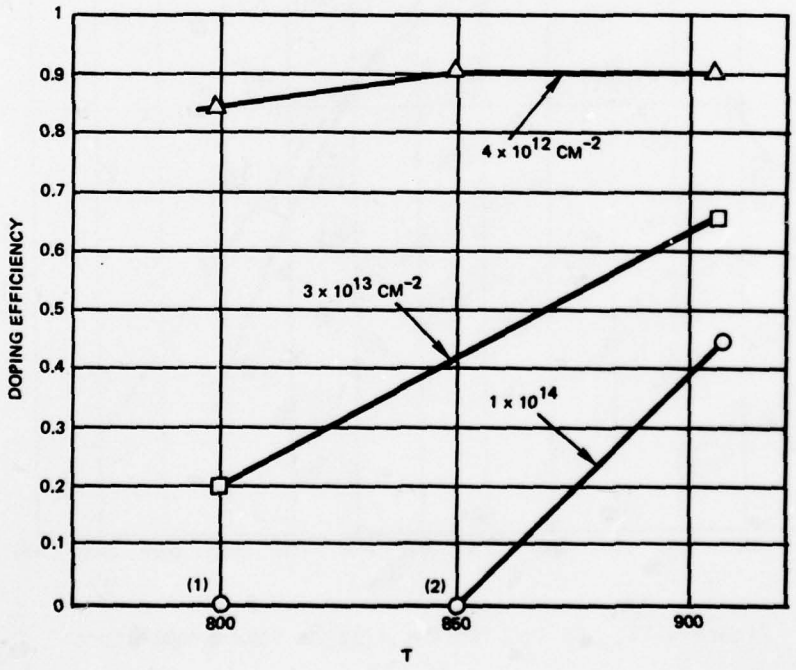


Figure 4-15. Doping Efficiency as a Function of Anneal Temperature for Various Doses

On the basis of these experiments, a low dose, low pinchoff voltage process has been developed which has sufficient uniformity and reprodicibility for the production of FET devices and ICs. This process can be easily upgraded for a semipilot line production.

TRW's ion implantation studies began early in 1977 on the 200 keV ion implant machine which was shared with the silicon processing laboratories. During the past 5 months all of the ion implantations have been performed with the new 400 keV ion implant machine, dedicated for the GaAs technology. This machine is shown in Figure 4-16.

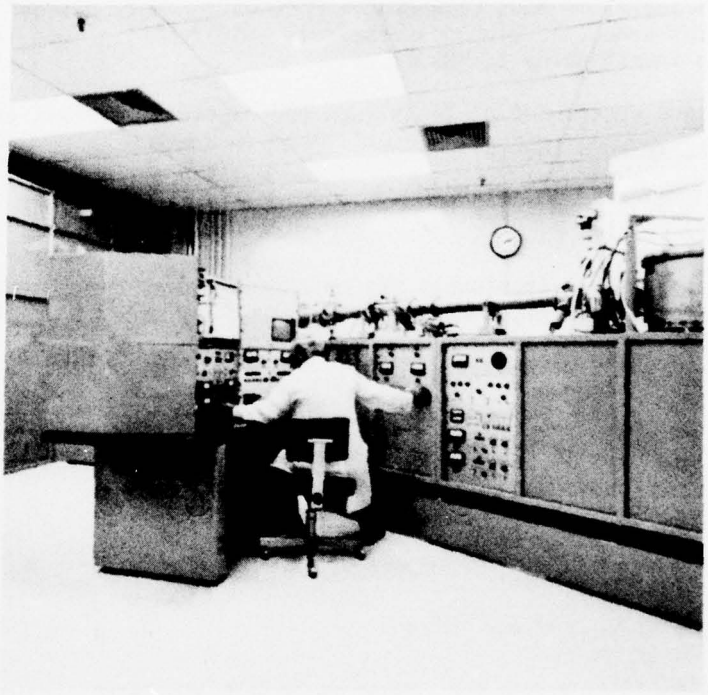


Figure 4-16. Photograph of 400 KeV Ion Implant Machine

One key to achieving the reproducible and controllable ion implantation process in GaAs was the extensive substrate material characterization and qualification procedure. The other key was the development of a good annealing cap.

4.2.4 Plasma Nitride Capping Development

Several techniques have been investigated to prevent crystal dissociation during the post implant anneal. These include nonencapsulating and encapsulating techniques. Nonencapsulating techniques include:

- Controlled atmosphere technique (CAT):[11] Consists of annealing the substrates in a high purity flowing hydrogen/arsenic atmosphere which is adjusted to be in near equilibrium with the implanted GaAs. TRW has performed cursory experiments in this area using arsine as the As source.

- Capless annealing technique. The GaAs wafers are annealed in a finely pulverized graphite layer mixed with crushed GaAs.

- Laser annealing.[12] Q-switched ruby lasers with 20 nsec pulses and 1 joule/cm^2 have been used. Most of the work has been directed towards annealing high dose implants ($\geq 10^{14} cm^{-2}$). This is also being investigated at TRW.

The various encapsulating techniques and capping materials used for annealing implanted GaAs include the following:

- SiO_2 - Sputtered
  - Pyrolytic
  - Spin on

  This was previously the most widely used cap; however, low doping efficiency and Ga permeabiltiy made it unsuitable

- Si_3N_4 - CVD
  - Sputtered
  - RF plasma

  Best cap for ion implant with processing ease

- AL_2O_3 - CVD

- AlN - Sputtered
  - Evaporated

- Ga_2O_3 - Thermal

TRW has investigated most of these materials and techniques and found that plasma-deposited nitride is the most successful in terms of performance and reproducibility. Except for the very early stages, plasma-deposited Si_3N_4 has been used exclusively in this program.

An effective encapsulant should be able to reliably protect the implanted GaAs surface from dissociation at temperatures up to at least 900°C. It should also be able to prevent outdiffusion of the implanted species. Improper encapsulation can result not only in low activation of the implanted species but also in anomalous carrier concentration profiles in the substrate. Changes at the substrate concentration profile may result in a reduction in the carrier concentration in the implanted layer. Outdiffusion of arsenic and/or gallium may produce nonstoichiometric layers in the surface of the GaAs.

Anomalous diffusion broadening effects observed in some implant profiles may be attributed to two factors:

- The influence of high background levels of compensating materials in the starting GaAs (e.g., Cr-doped semi-insulating substrate)
- The interdiffusion effects between the constituents of the dielectric encapsulant and the implanted layer.

These difficulties led to the search for nonencapsulating techniques. These are in their infancy, and although in principle offer some advantage over the encapsulating techniques, much work is required before they can be implemented successfully. Therefore, only encapsulating techniques have been used on this program.

Implant results with Si_3N_4 have shown a strong dependence on both the method used to deposit the Si_3N_4 and the particular deposition parameters. Sputtered Si_3N_4 (primarily reactively sputtered), RF plasma deposited Si_3N_4, and pyrolytic Si_3N_4 have all been used. Sputtered Si_3N_4 varies substantially from one laboratory to another, and sometimes has a tendency to bubble and peel off the wafer at high anneal temperature. Pyrolytic Si_3N_4 has been used successfully, but has the disadvantage of requiring high deposition temperatures.

The most promising encapsulating technique appears to be RF plasma-deposited Si_3N_4. This has been described by other laboratories and extensively developed at TRW. The salient features of TRW's RF plasma nitride system are as follows.

- Film properties
  - Low porosity
  - Adheres to GaAs at anneal temperatures up to 900°C
  - Deposited at low temperatures (275° to 400°C)
  - Doesn't dissolve Ga or As (stoichiometric interface).
- Implantation annealing properties
  - Reproducible ion implanted profiles
  - High doping efficiencies for low dose silicon ion implants ($3 \times 10^{12} cm^{-2}$)
  - High concentration N+ layers ($4 \times 10^{18} cm^{-2}$) for high dose silicon implants.

Using this RF plasma nitride encapsulation, a reproducible ion implantation process has been developed by TRW.

The silicon nitride used at TRW as the cap for annealing ion implanted wafers is deposited by the low temperature <400°C reaction of silane and nitrogen in an RF plasma. It has been reported[13] that if the nitrogen is introduced at the top of

the reaction chamber, goes through an RF coil, and then mixes with silane just above the heated wafers, the resultant deposit will not contain a significant amount of oxygen. It is important to minimize the oxygen in the cap because it causes gallium vacancies to form at the anneal temperature. Therefore, our first attempt was to duplicate the system described by Helix, Vaidyanathan, and Streetman.[14]

The system design began with a basic vacuum system pumping station with a 6-inch diffusion pump to which a 6-inch diameter x 24-inch high bell jar was added. Initially a 2-inch substrate heater stage which fits at the bottom of the bell jar was used. This was subsequently changed for a 3-inch heater to improve uniformity. Some experimenting was necessary to scale to the large heater stage. This included changing the dispersion ring as well as the gas flow composition. The bell jar was designed so that the nitrogen could be introduced at the top of the bell jar and passed between the RF coils as shown in Figure 4-17. The RF coil is wound around the bell jar between the nitrogen inlet and the silane dispersion ring. The silane dispersion ring is designed to have the same diameter as the substrate heater stage. The silane is introduced into the system through this dispersion ring, just above heater stage. Figure 4-18 is a photograph of the final system.

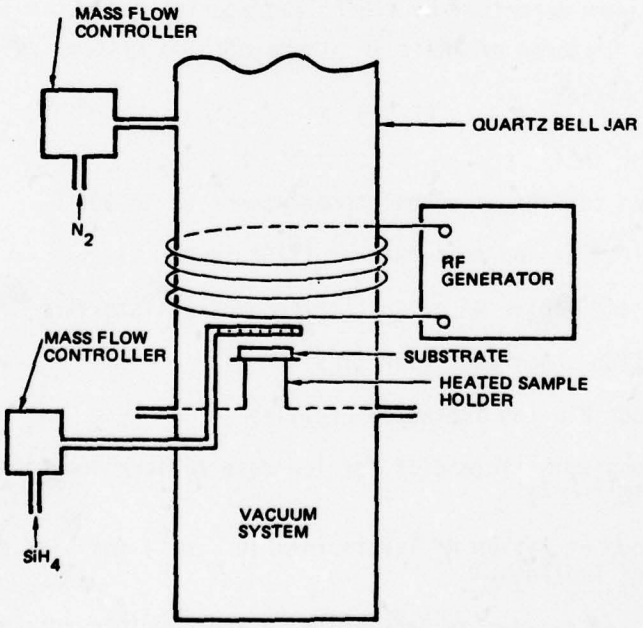


Figure 4-17. RF Plasma Nitride Deposition System

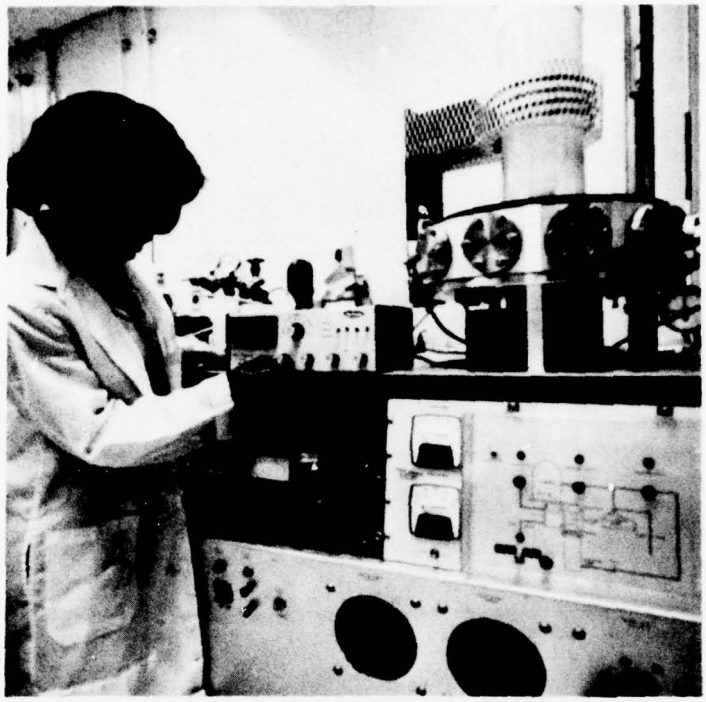


Figure 4-18. Photograph of Plasma Nitride Deposition System

A mixture of 2% silane in argon is used for the silane source. The gas flows are controlled by mass flow controllers. The RF power supply is a 600 watt unit operating at 27 MHz. The operating pressure is read on a thermocouple gauge. For most of the depositions, the heater temperature was maintained at 365 ±5°C. The system is initially evacuated into the 10^{-6} Torr range with the diffusion pump to reduce the background water and air pressure. Then the roughing pump is used for the actual run.

Initial runs in the 2-inch heater system were made using 15 cc/min of 2% SiH_4 in Ar and 24 cc/min nitrogen. However, due to the low (<50 μm) operating pressure in this setup, the deposition rates were low and the index of refraction was 1.8 to 1.9. Therefore, the flows were gradually changed until the 2% SiH_4 was 40 cc/min and the N_2 was 10 cc/min. A typical plot is shown in Figure 4-19 for film refractive index vs 2% SiH_4 flow for various flow ratios of SiH_4/N_2 for both the 2-inch diameter and the 3-inch diameter systems. Higher flow rates with a lower nitrogen concentration were required to maintain the uniformity and refractive index that was obtained with the 2-inch diameter system.

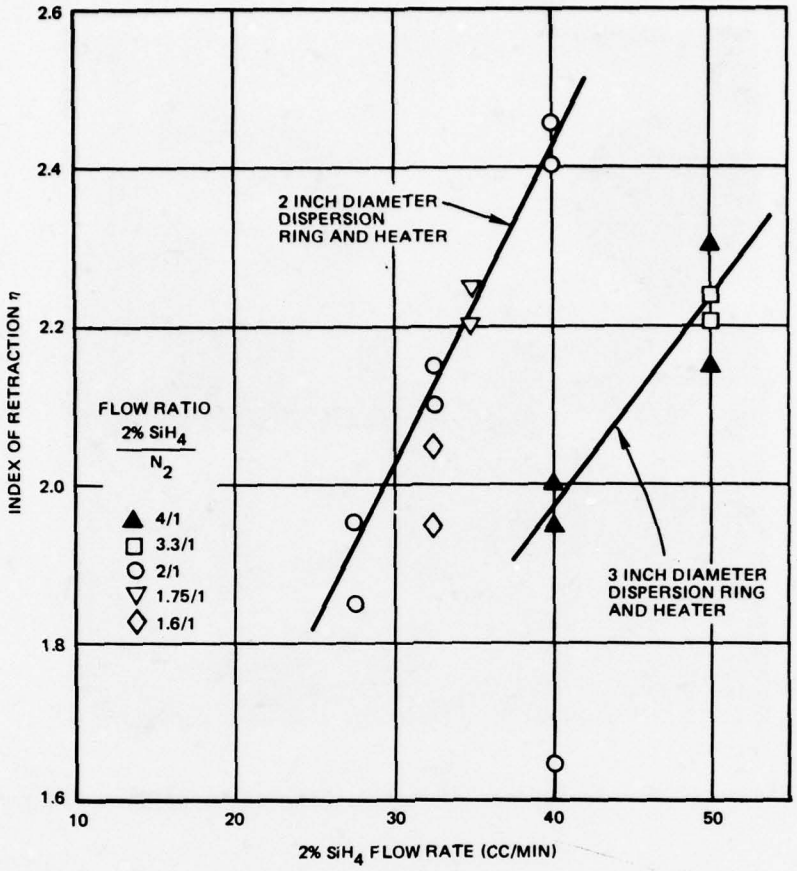


Figure 4-19. Index of Refraction of Plasma Nitride as a Function of Gas Flows and System Geometry

The present deposition rate is approximately 85 to 90 Å/min with SiH_4 flow of 47 cc/min and N_2 of 11 cc/min. To achieve reproducible results, it is necessary to monitor the initial gas pressures and the gas pressures following the introduction of N_2 and SiH_4 into the deposition chamber. Variations in gas pressure on the mass flow meters may be caused by an inadvertent leak or clogging of the flow meter bypass. In the initial system design, RF interference caused variations in the mass flow meters. This was alleviated with proper shielding of the controllers and their power supply.

One problem with encapsulating GaAs with Si_3N_4 is the high interfacial stress due to mismatch in thermal expansion coefficients between GaAs and Si_3N_4. When the stress exceeds the maximum breaking stress, mechanical failure results. In our process, the Si_3N_4 films are covered with low temperature deposited SiO_2 for improving the physical integrity of the film; the effective maximum tearing stress has been observed to increase in the Si_3N_4/SiO_2 sandwich structure. Experiments were conducted to find the optimum $Si_3N_4/SiO2$ film thickness configuration. The Si_3N_4 films

were varied from 500 Å to 10,000 Å. The best combination, for a compromise between film stress and protective quality, is 900 Å, Si_3N_4/4000 Å SiO_2. Films deposited by this technique at TRW have held up well to anneal temperatures above 900°C. This has been demonstrated on a series of over 100 wafers with implant doses ranging up to $10^{15} cm^{-2}$.

4.2.5 Device and Circuit Fabrication

The basic technologies described in Section 4.1 as well as the new developments of Section 4.2 were used to establish a processing sequence suitable for fabricating both discrete devices (FETs and TEDs) and integrated circuits. The primary objective in fabricating the discrete devices was to provide a vehicle to measure device improvement and to provide parametric data for device and circuit modelling.

During the early stages of the program, the available MESFET models were employed. The earlier models, although not as comprehensive as the present model, indicated that the primary device concerns in integrated circuit development were minimizing device parasitics and reducing the transit length of the device carriers. The vehicles used in this development were 1 μm gate MESFETs and TEDs. These device structures are shown in Figure 4-20. The MESFETs had a gate width of 250 μm and 1 μm separation from source-to-gate and gate-to-drain. The TEDs had a cathode-to-gate spacing of 3 μm and an anode-to-gate spacing of 20 and 10 μm. These anode-to-gate spacings set the transit length frequency at 5 and 10 GHz, respectively.

The masks for these devices were fabricated on a company sponsored program. The technology developed was aimed toward improving device performance and circuit yield. The MESFETs and TEDs were fabricated using the conditions shown in Table 4-4.

Table 4-4. MESFET and TED Parameters

Device	N	X	N+	Epi Buffer	Ion Implant
MESFETs	1 to 2 x 10^{17} cm^{-3}	0.15 to 0.30 x 10^{-4} cm	No	Yes	Yes
TEDs	3 to 5 x 10^{16} cm^{-3}	0.6 to 1.0 x 10^{-4} cm	Yes	Yes	No

High concentration N+ contacts were used with the TED devices to improve the specific contact resistance; a few MESFET devices were also fabricated with N+ ion implants in the ohmic contact region. Contact resistance values varying from 10^{-5} to 10^{-6} Ω-cm^2 are dependent on the cleaning procedure prior to metal deposition and

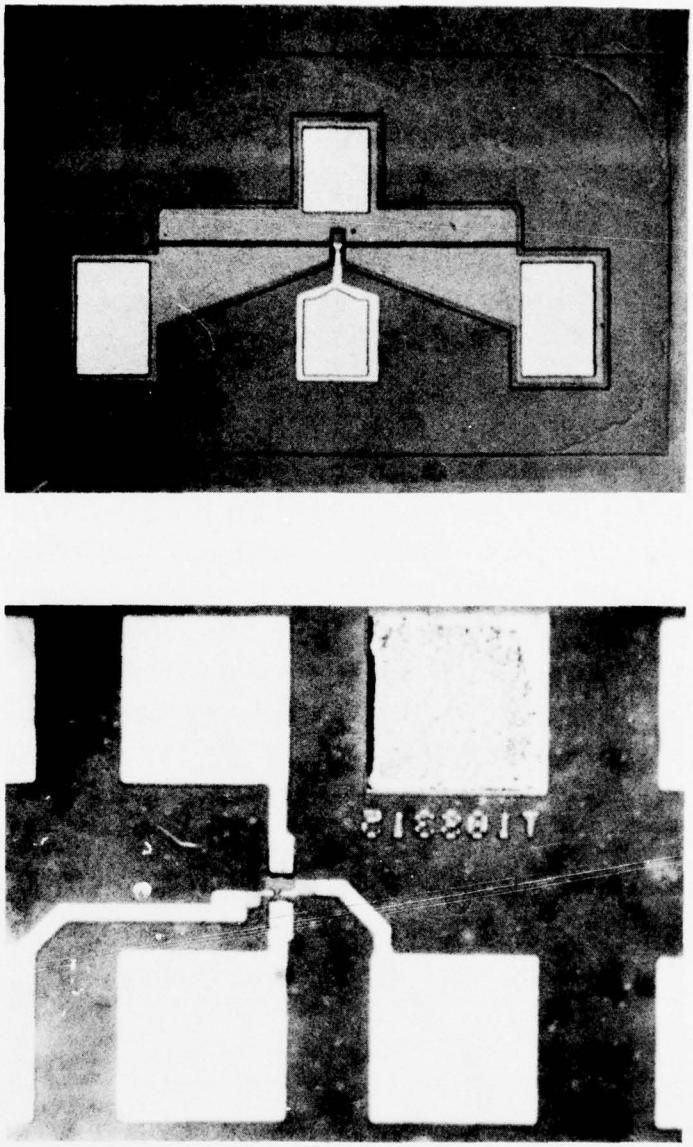


Figure 4-20. TEDs and FET Test Devices

the metal contact sintering conditions. The distribution of the specific contact resistance from a series of test devices on wafer D-23 is shown in Figure 4-21. This wafer was sintered at 460°C in hydrogen for 3 minutes. Another wafer lot sintered only 1.5 minutes had about an order of magnitude higher specific contact resistance.

There is an improvement in contact resistance when an N+ layer is used in the contact region. Figure 4-22 shows examples of six wafers used to evaluate contact resistance. Wafer numbers 2, 3, and 6 were N-type wafers with no N+ layer in the ohmic contacts. Wafer numbers 4, 5, and 7 had an N+ layer in the contact region. The epitaxial layer concentration was 1×10^{17} cm^{-3} in the case of the 1st three samples. Sample number 2 was sintered 1.5 minutes at 465°C. Samples 3 and 6 were sintered 3 minutes.

It has been noted that sintering times can vary depending on the thermal mass of the wafer holder used in the sintering furnace. Samples 4 and 5 were measured without etching away the N+ layer between the contacts. The plots shown in this figure were generated from resistance measurements of ohmic contacts separated by various distances from each other. The resistance is plotted as a function of distance and the values extrapolated to the intercept give the contact resistance. The slope of the lines gives the resistance due to the doping concentration in the semiconductor. Since sample number 7 had the N+ layer between the contacts removed by etching, the slope is different from the slopes of samples 4 and 5.

The N+ layers investigated have been fabricated by two techniques: N+ epi deposition and high dose ion implantation. TEDs fabricated on this program have used ion implanted N+ contacts where the peak concentration has been in the range of 6×10^{17}-$4 \times 10^{18} cm^{-3}$.

The processing sequence for TEDs is shown in Figure 4-23. The TEDs were fabricated using boron implant isolation rather than our standard mesa process. The N+ contact process when used with the boron implant isolation process gives a larger number of processing steps. An aluminum film is used to mask against the high dose N+ implant.

The boron isolation technique has been successfully developed in our laboratory. This implant is made after annealing the N+ implants, but requires a high temperature treatment at about 550°C to minimize the surface conduction. This B ion when implanted at 400 keV, requires a mask of about 1 μm thickness of Au. Planar TEDs with B+ isolation have been demonstrated.

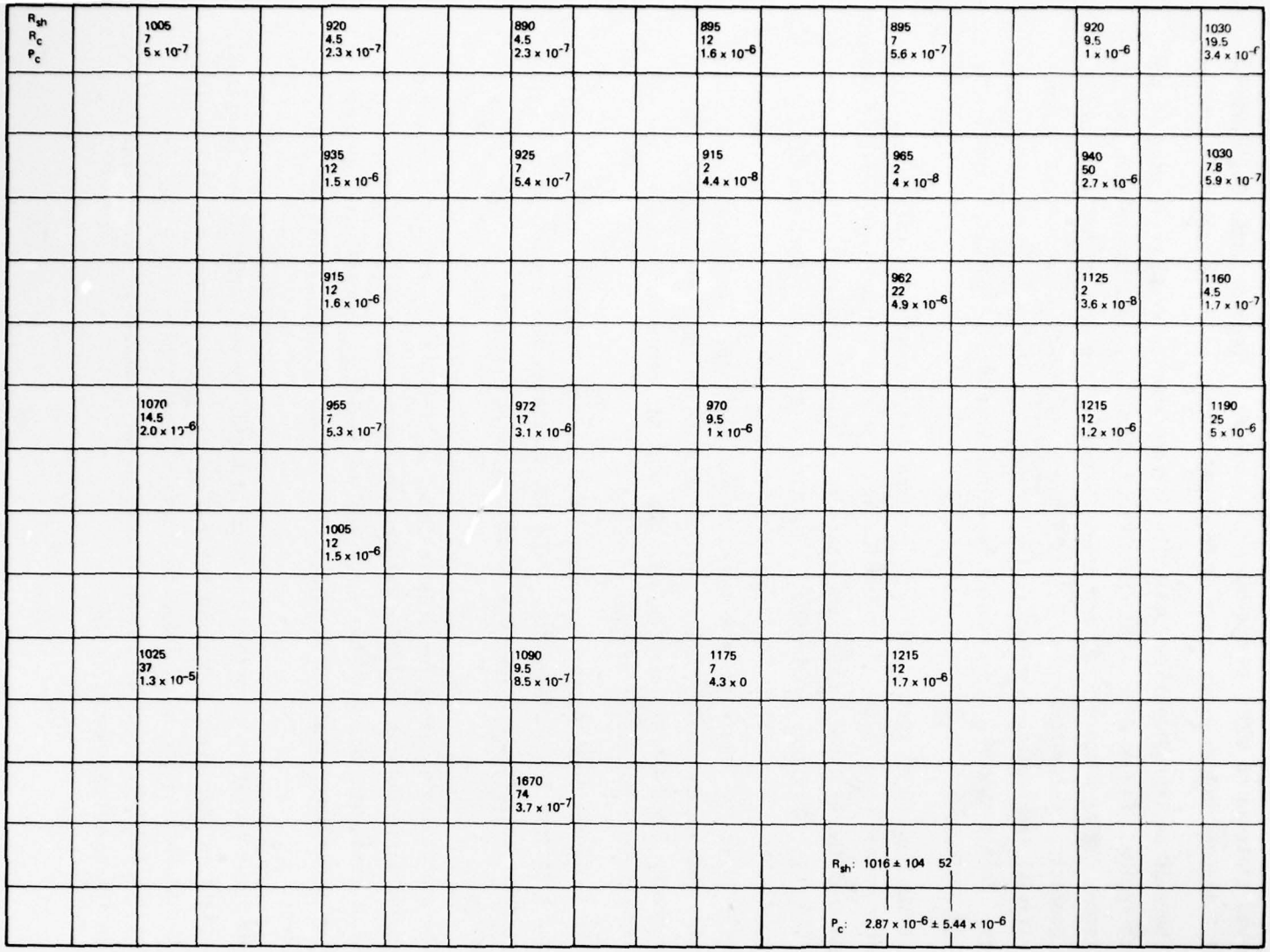


Figure 4-21. Specific Contact Resistance

AD-A079 588 TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CA F/G 9/5
GAAS ANALOG INTEGRATED CIRCUITS (GAAS RF-LSI). PHASE I. PROGRES--ETC(U)
AUG 79 N00039-78-C-0305
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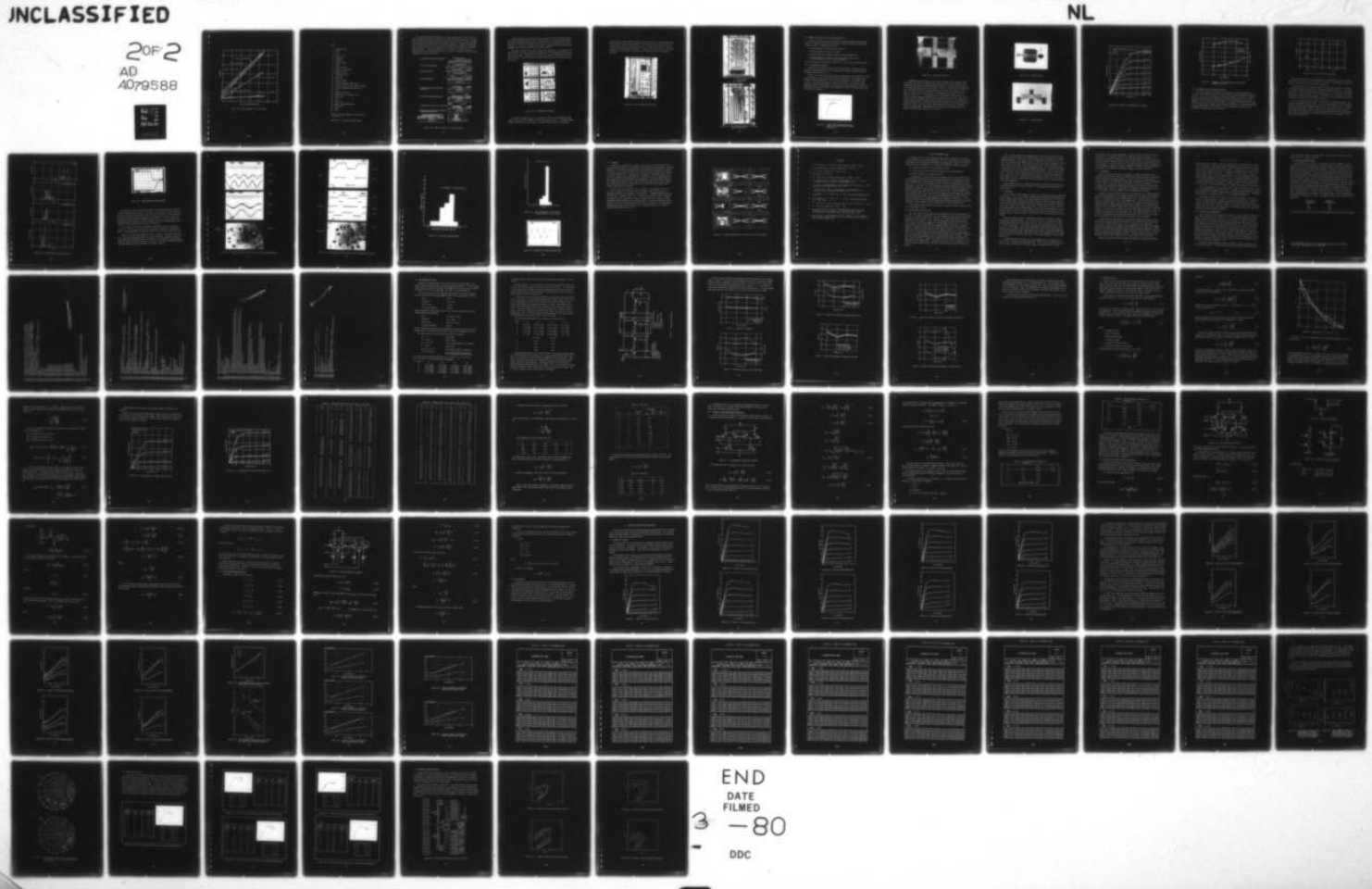

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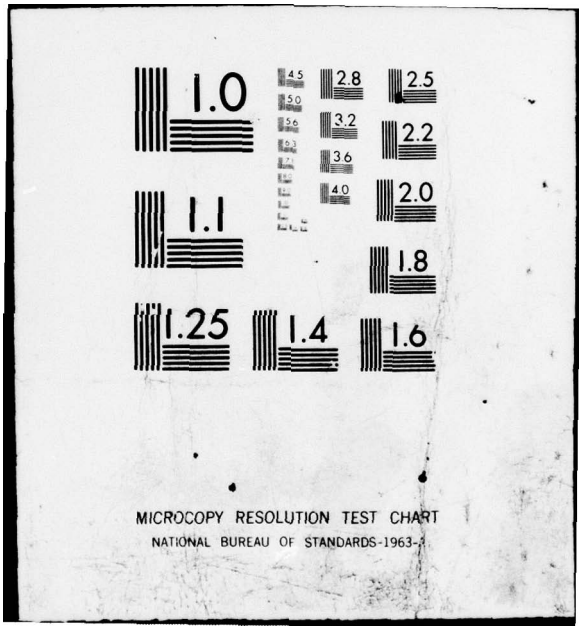
1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
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4.5
5.0
5.6
6.3
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

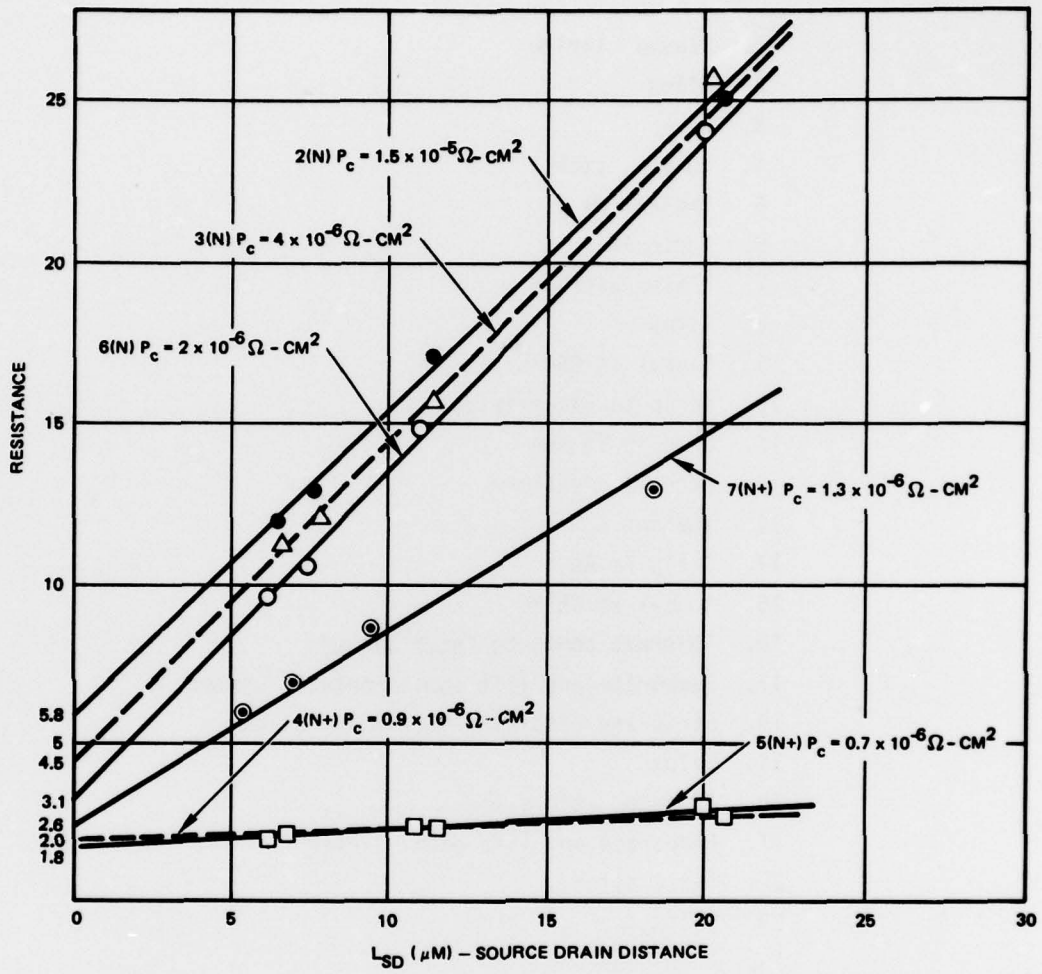


Figure 4-22. Au/Ge (Eutectic) + Ni + Au System

Step

1. Plasma nitride
2. Silox
3. Al
4. PR N+ etch
5. Implant N+
6. Strip Al
7. Plasma nitride
8. Silox
9. Anneal at 850°C
10. Strip to 1st nitride
11. Deposit Ti Au*
12. Etch mesa pattern
13. Implant B
14. Strip Ti Au
15. Anneal at 550°C
16. PR ohmic contacts (etch silox)
17. Evaporate and lift ohmic contact, sinter
18. Strip any remaining nitride or silox
19. Silox
20. PR gate, etch silox
21. Evaporate and lift gate, sinter
22. Strip silox
23. Silox
24. Open vias
25. Deposit interconnect metal
26. PR and etch
27. Sinter
28. Test

*If N+ is not used, deposit silox and proceed from Step 11.

Figure 4-23. N+ Planar TED Process Flow

The processing sequence for MESFETs is shown in Figure 4-24. FETs on this program have been fabricated using epi material and with ion implanted wafers. The epitaxial layers were deposited on epitaxial buffer layers while the ion implanted FETs were made with direct implant into the Cr-doped substrates. In general, the MESFETs were not fabricated with N+ contact implants, although a few samples were evaluated with N+ implants. The primary emphasis in this area was to concentrate on the repeatability of the lithography techniques to resolve 1 μm gates and improve the FET processing for better gate control.

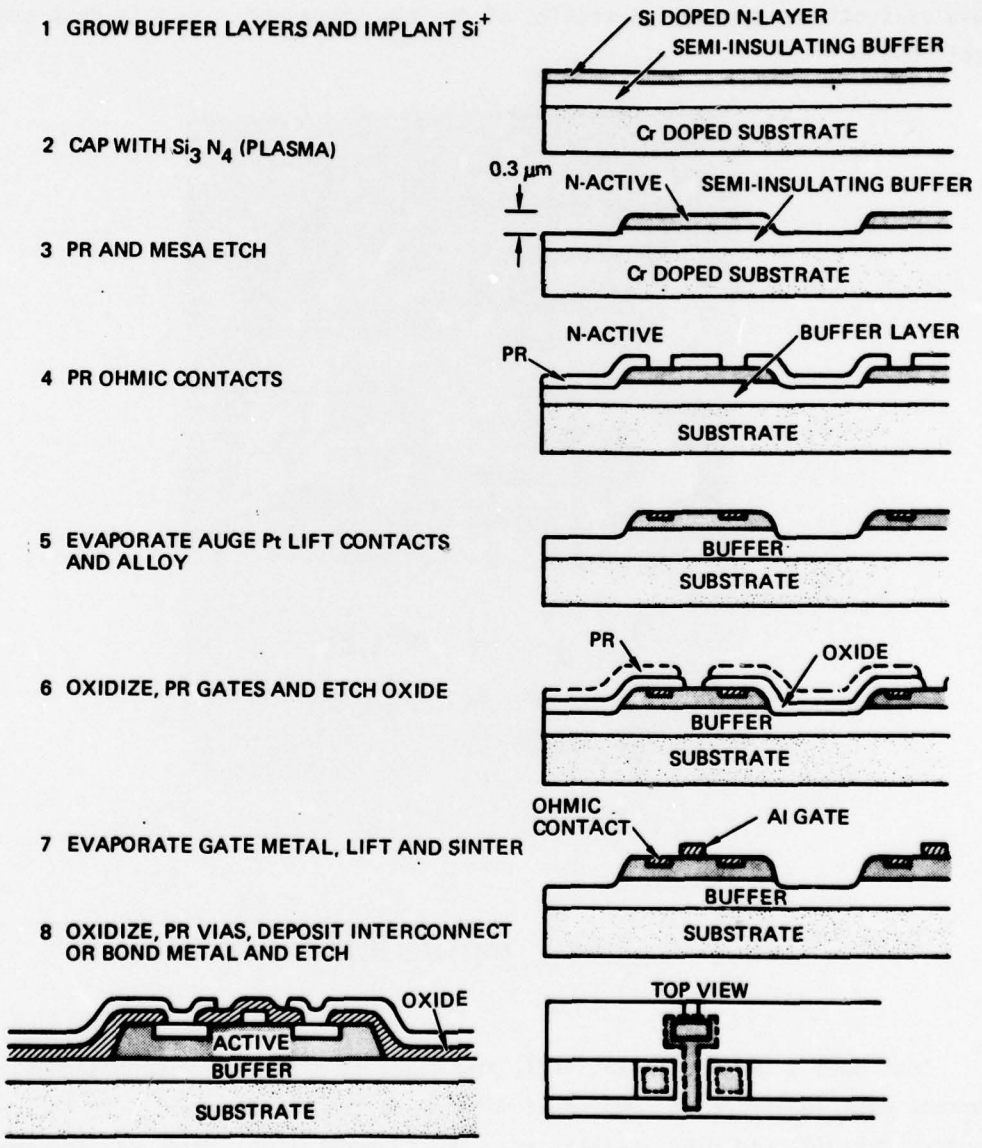


Figure 4-24. MESFET and GaAs IC Flow Chart Diagram

These technologies have been applied to two practical circuit chips fabricated from existing integrated circuit masks. These masks were not developed for this program and the material parameters were not typical for that required for the analog multipliers. The circuits, however, were useful in developing the process and device parameter controls which are necessary for the multiplier.

Test mask 1 (Figure 4-25) is the analog/digital test mask. It includes FET differential pairs for device studies and a sample and hold and comparator circuit with output buffer stages. Additionally, this mask has a series of test vehicles for process evaluation. Evaluation results of devices processed from this mask are given in Section 4.3.

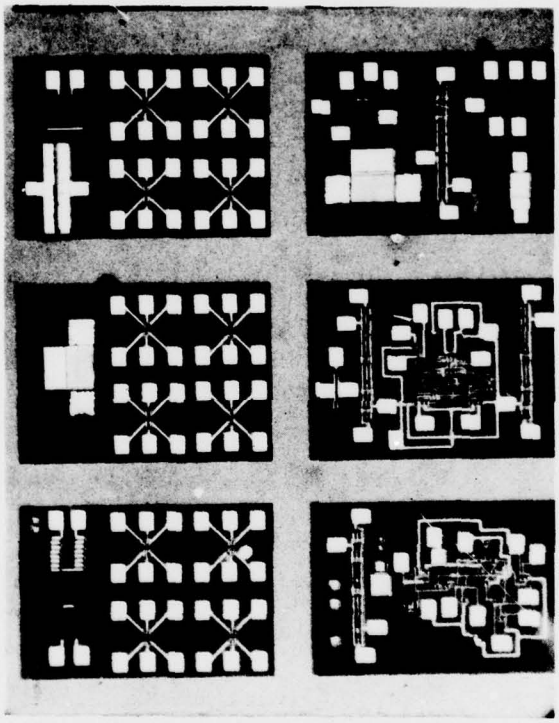


Figure 4-25. Analog/Digital Test Mask

Test mask 2 (Figures 4-26, 4-27, and 4-28) is a digital mask designed to study current mode logic and to compare it with diode transistor logic. It includes several counter circuits and ring oscillators. The purpose of this mask was to generate

circuits with a higher integration level and provide a means for evaluating the GaAs material device and processing parameters. Besides the series of counter circuits and frequency dividers, this mask has a series of identical devices in a string for evaluating device and process uniformity. Processing with this mask was only initiated within the past month and therefore only limited test results are presently available.

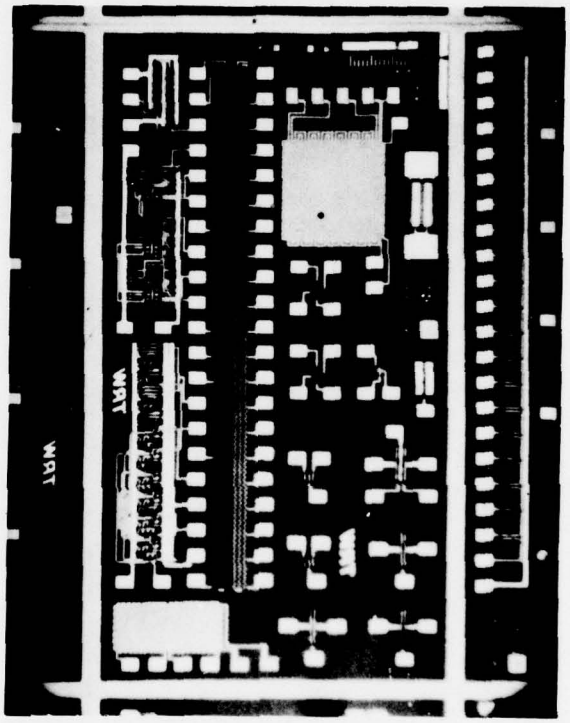


Figure 4-26. Current Mode Logic Test Mask

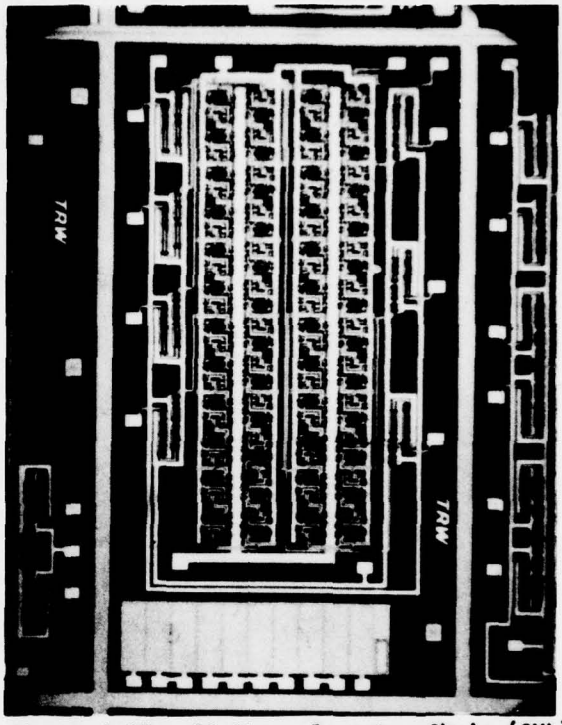


Figure 4-27. 48-Stage Inverter Chain (CML)

A - 2 Level Metals
B - Capacitors

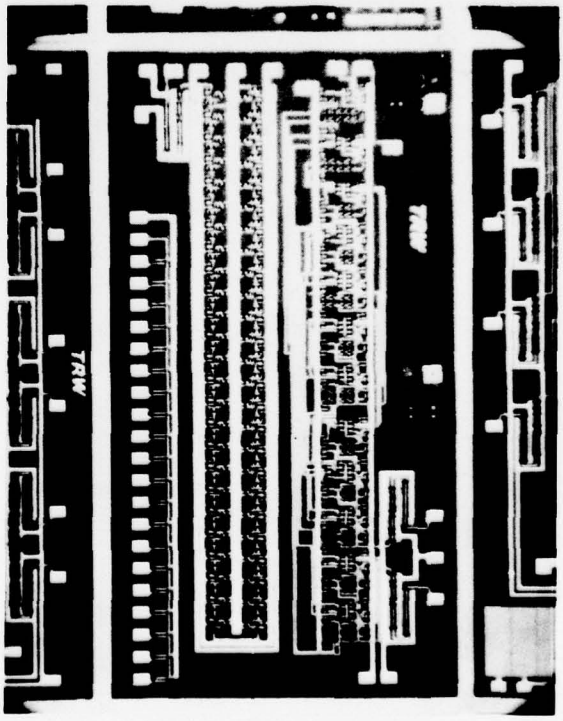


Figure 4-28. 49-Stage Ring Oscillator (SDL) Dual Modulus Counter (CML)

4.3 SUMMARY OF DEVICE AND CIRCUIT PROCESSING RESULTS

During this program, we have successfully developed several key process technologies and have used these to fabricate high performance devices and integrated circuits. Specific accomplishments include:

- Fabricated planar TEDs using boron isolation
- Fabricated MESFETs with gain to 18 GHz
- Measured data which compares favorably with the computed data
- Demonstrated yield capability for uniform devices across a wafer and the capability for up to 100 gate complexity

The discrete device and integrated circuit data is given in the following sections.

4.3.1 Discrete Device Results

There were three primary objectives in fabricating TEDs: show planar device structure, develop capability for N+ implantation for contact resistance reduction, and demonstrate anodization trim.

Several lots of TEDs were fabricated which demonstrated the N+ technology, planar boron isolation, and the combination of the two technologies. The existing 5 and 10 GHz TED masks were employed. Typical device characteristics are shown in Figure 4-29. The same type of device is shown in Figure 4-30. The results compare favorably with earlier measurements on mesa TEDs, as shown previously in Figure 4-3. Anodization trim was not applied in this experiment, since the epi wafers were grown to the desired thickness.

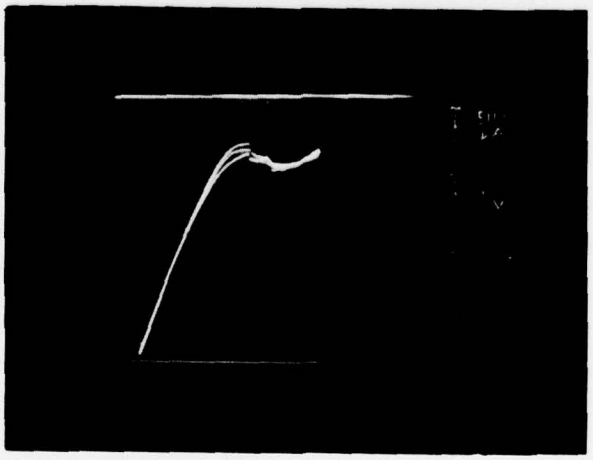


Figure 4-29. Typical Device Characteristic for Planar, N+ 10 GHz TED with 15 Micron Wide Channel

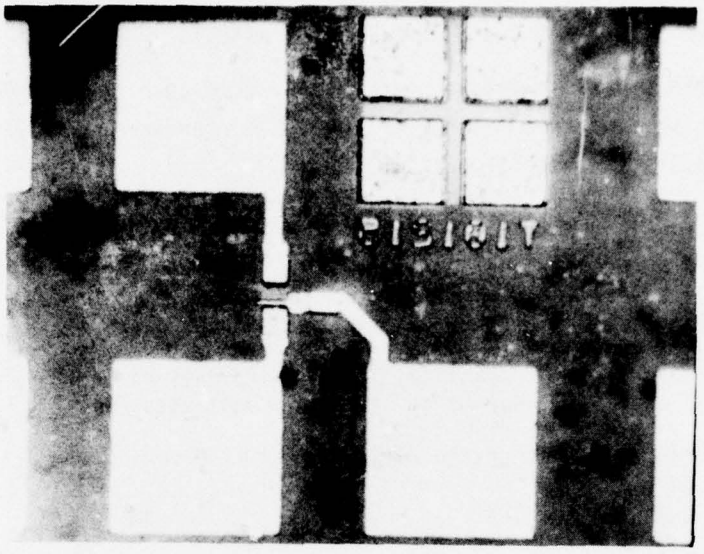


Figure 4-30. Planar, N+ 10 GHz TED

The MESFETs were fabricated to verify the device models and to compare the discrete device fabrication. The MESFETs developed during the past few months are of a different design from that used and reported on earlier. The primary differences are in the gate configuration and the gate width. The earlier version shown in Figure 4-31 had a gate width of 300 μm with the configuration of two parallel gates of 150 μm each. The later version has the gate in a T-shape with a gate width of 250 μm as shown in Figure 4-32. The T-shaped device has the potential of lower parasitics. Typical dc characteristics from these devices are given in Figure 4-33. The gain and noise figure of the T-shaped devices are presented in Figure 4-34, and compared with computer generated data. The 250 μm devices have 2 dB gain at 18 GHz while the earlier devices had a gain of 1 dB at 13 GHz. About nine wafer lots have been processed with this T-shaped mask. Measurement data from these devices and comparisons with computer predicted results were given in Section 2.

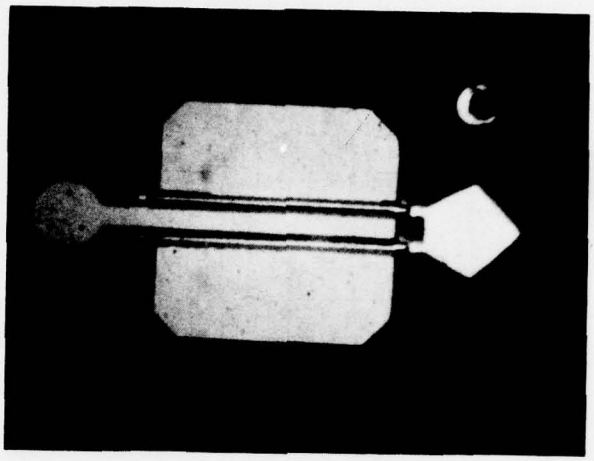


Figure 4-31. Parallel Gate FET

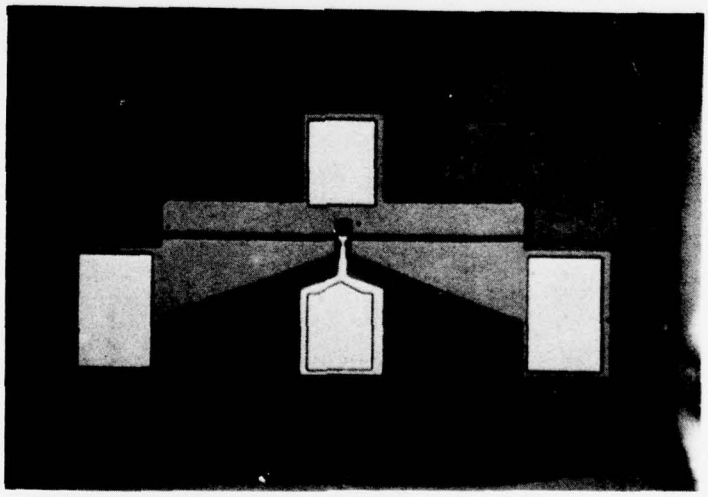


Figure 4-32. T-Shaped Gate FET

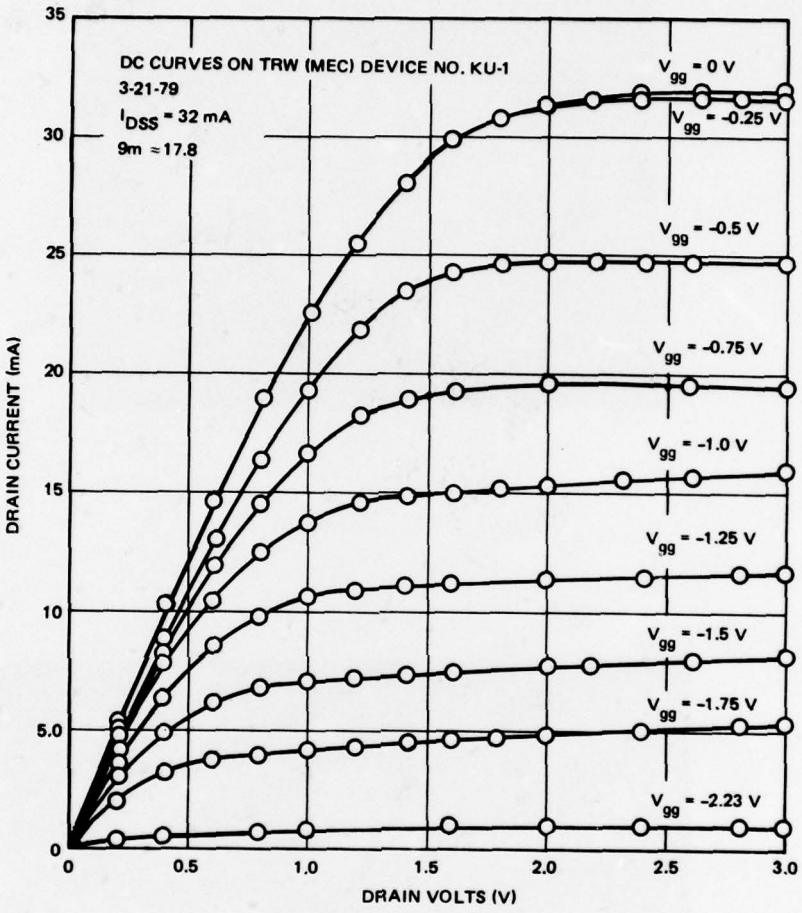


Figure 4-33. Typical DC Characteristics of MESFETS

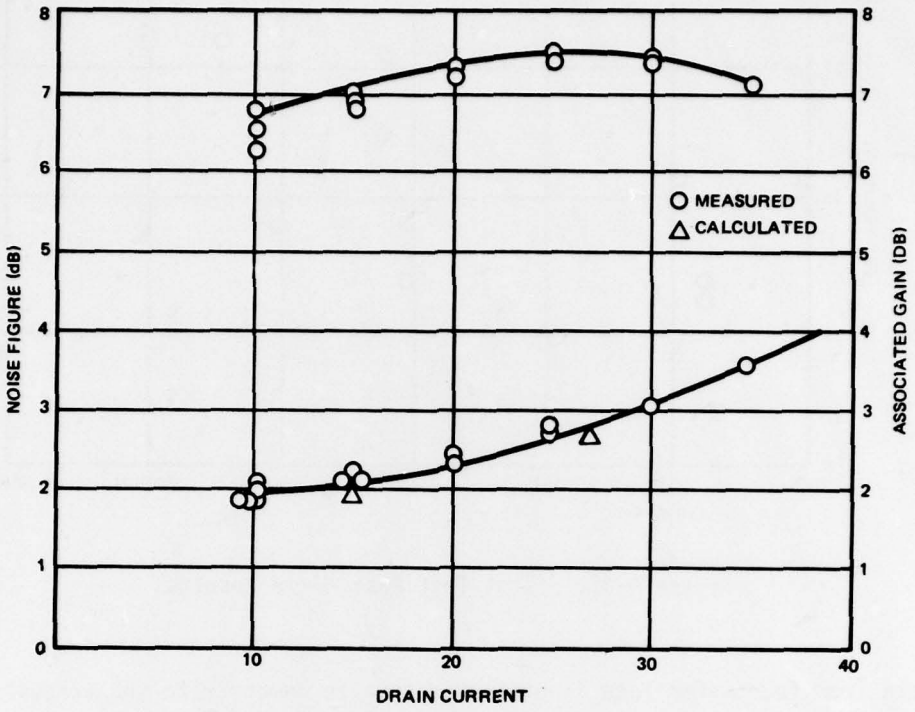


Figure 4-34. Measured and Calculated Gain and Noise Figure of MESFETs at 4 GHz

4.3.2 Integrated Circuit Development Results

The process development using the two integrated circuit masks described in Section 4.2 has yielded a repeatable process for fabricating ion-implanted integrated circuits. The first test mask used for developing matched pairs of FETs has demonstrated a significant yield improvement which has been accomplished over the past 5 months. This yield chart, shown in Figure 4-35, indicates that the yield goes from 20% up to 80% over this period. Greater than 10% mismatch was considered unacceptable. The yield improvement is attributed to ion implant repeatability, ohmic contact improvement, and general process discipline.

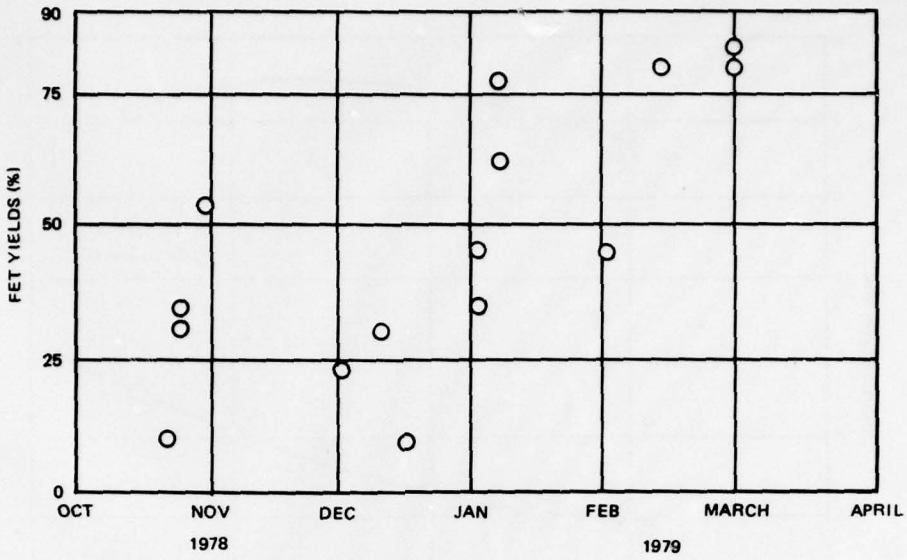


Figure 4-35. First Test Mask Yield Results

Data from four wafer lots is presented here to demonstrate the process achievements. These are wafer lots D-18, D-23, D-24, and D-25. The pinchoff voltage distribution for the various lots is plotted in Figure 4-36.

The distribution in the measured pinchoff voltage across the wafer is a measure of the gate characteristics as well as the dopant concentration profile. The improvement from lot D-18 to lot D23A may be attributed to the use of good qualified material in D-23A and marginal material in D-18. The improved V_p in lot D-24 over D-23A may be attributed to improved process techniques. Wafer lot D-25 was processed concurrently with lot D-24, and had a similar standard deviation.

Circuits fabricated with this mask included MESFET and Schottky NOR gates, comparators, and sample and hold circuits. These circuits operated well at low frequency but were limited in high frequency operation by the output buffer circuits. A typical waveform of the NOR gate is shown in Figure 4-37. This NOR gate with the output buffer shows 15 nsec delay time. The low frequency characteristics of the sample and hold and the strobe comparator one depicted along with the chip photographs in Figures 4-38 and Figure 4-39.

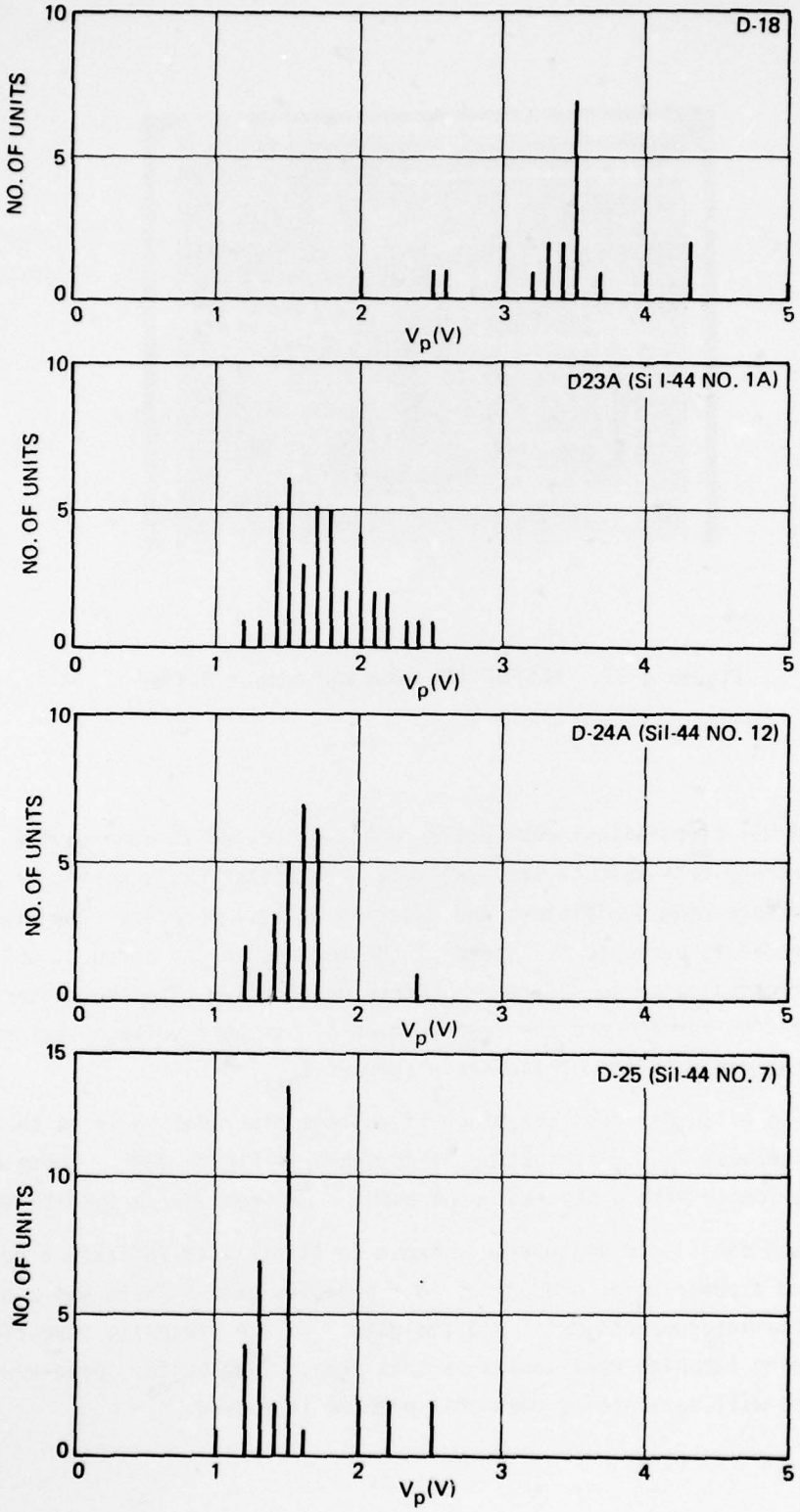


Figure 4-36. V_p Distribution on Four Wafer Lots

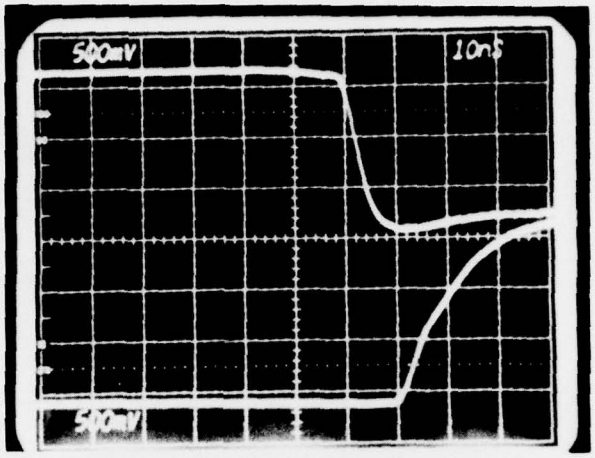
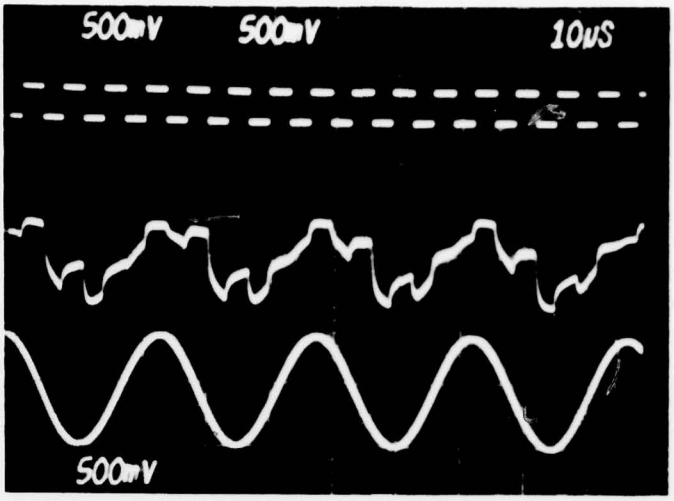


Figure 4-37. MESFET NOR Gate and Output Buffer

The second MSI circuit test mask was recently processed through device fabrication and preliminary test results are available. This mask has a series of counter circuits, a 49-stage ring oscillator, and a string of test devices. The ring oscillator has been tested to evaluate the speed of the devices in the circuit, while the test devices were evaluated to determine process uniformity. The two criteria for measuring process uniformity are the distribution of pinchoff voltage measured across the wafer and the distribution of the drain current I_{dss}.

For a string of 20 devices, the pinchoff voltage distribution is as shown in Figure 4-40. The best I_{dss} distribution is as shown in Figure 4-41. These devices had a 1 μm gate length with a separation of about 2 μm from source-to-gate and gate-

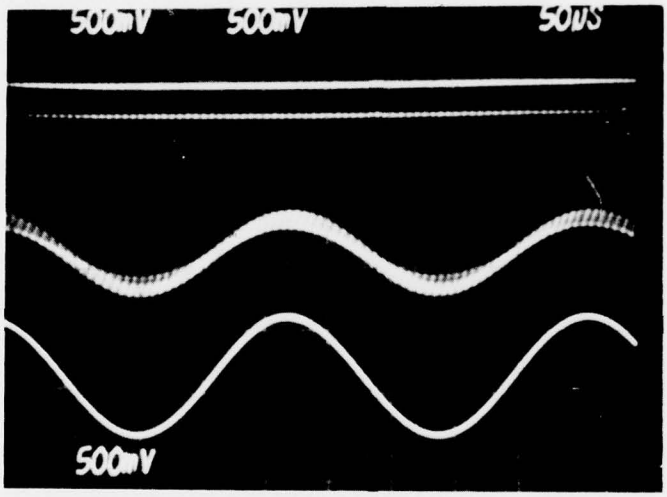
Typical ring oscillator measurements shown in Figure 4-42 indicate a delay time of ≈1.1 nsec and a power-delay product of ≈0.5 p-joules/gate. There was a high resistance between the interconnect metal and the gate. We are presently investigating means for reducing the high resistances in this area. Even better speed-power products and higher speed will be achieved when this problem is solved.



STROBE

OUTPUT

INPUT

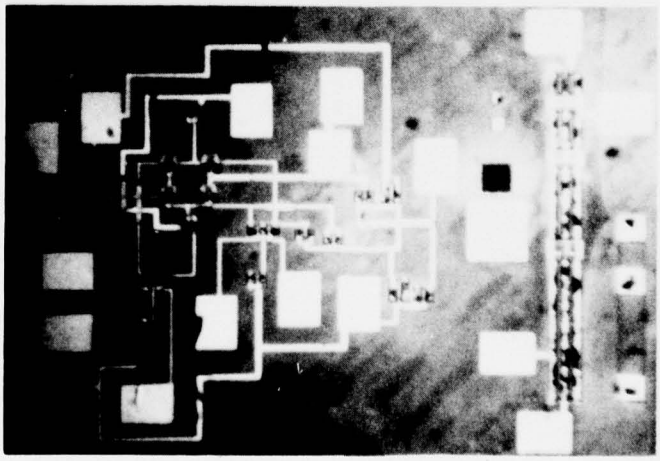


STROBE

OUTPUT

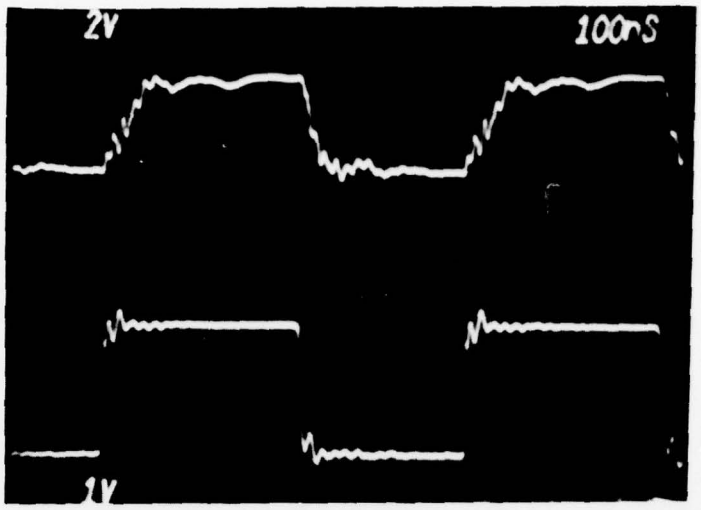
INPUT

SAMPLE
& HOLD



BUFFER

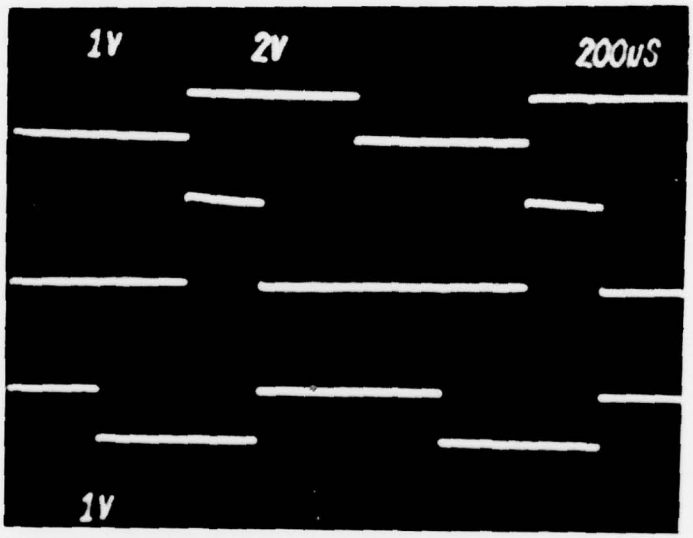
Figure 4-38. Sample-and-Hold Circuit Low Frequency Chip Characterization



BUFFER

OUTPUT

INPUT

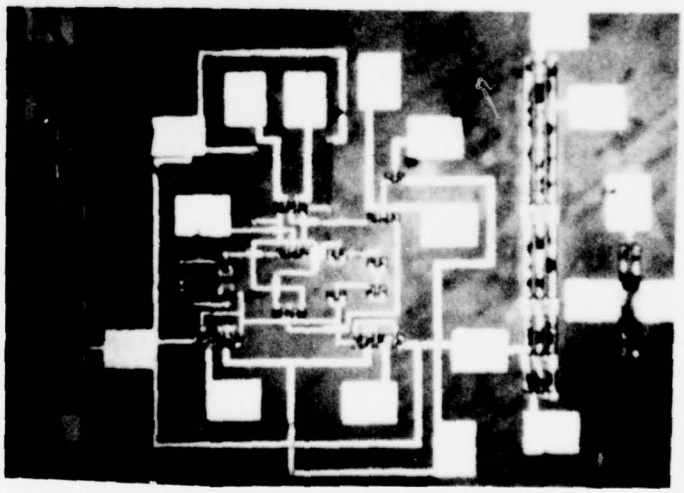


COMPARATOR

INPUT

OUTPUT

CLOCK



COMPARATOR

BUFFER

Figure 4-39. Low Frequency Characterization Buffer and Comparator Circuits

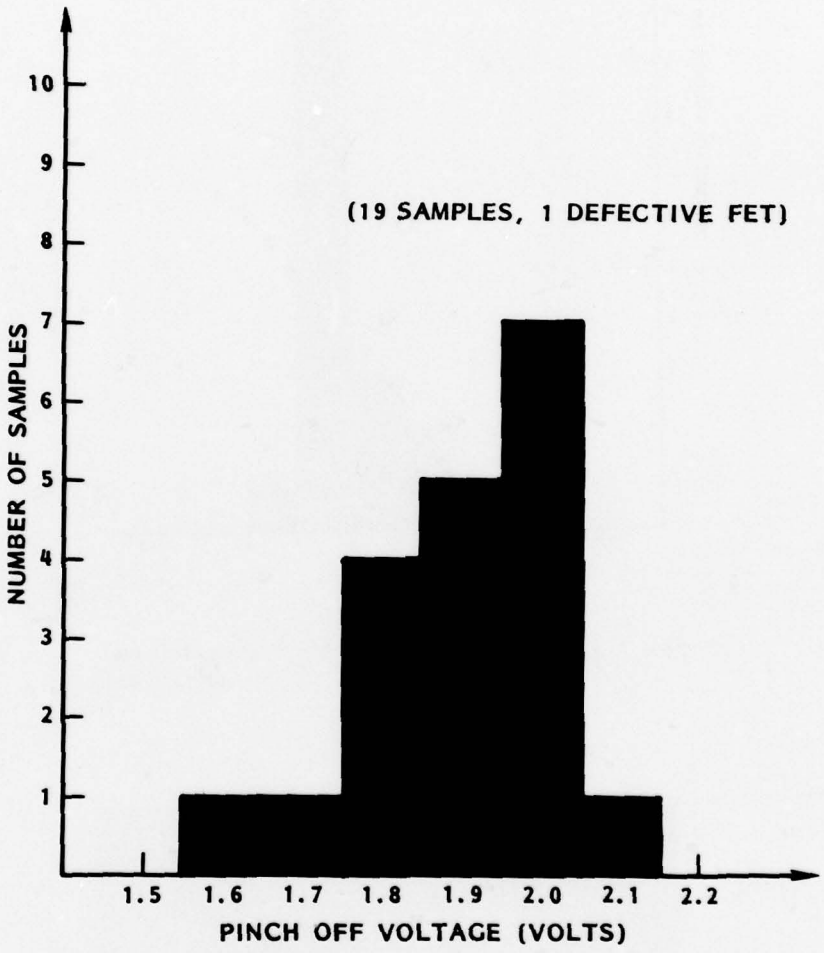


Figure 4-40. Pinchoff Voltage Histogram

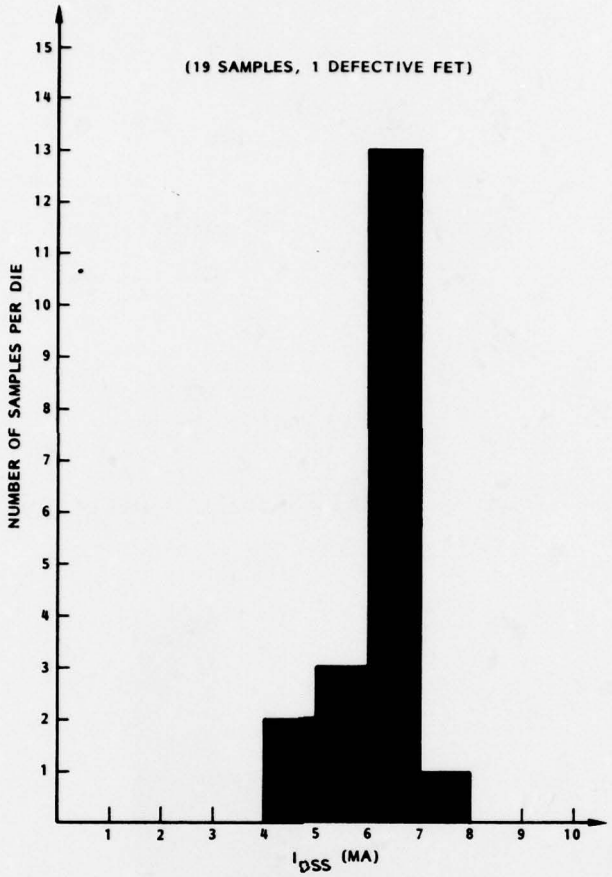


Figure 4-41. I_{dss} Histogram for 1 μm x 100 μm (20 FETs Spaced on 150 μm Centers)

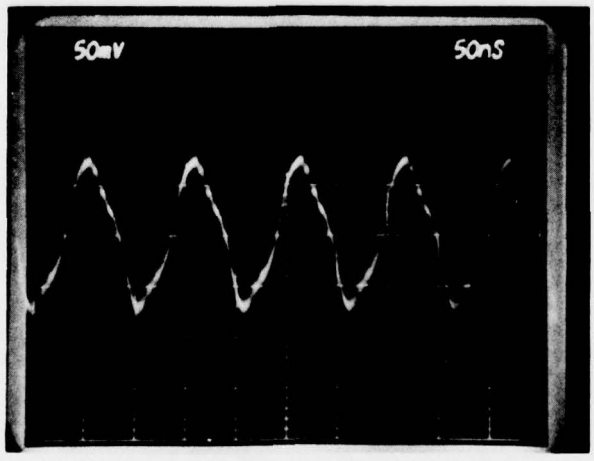


Figure 4-42. Waveform of 49-Stage Ring Oscillator

4.3.3 Summary

During the first phase of the program, TRW has demonstrated the capability for processing discrete devices and integrated circuits which are state-of-the-art for GaAs technology. The substrate characterization and qualification technique, the plasma nitride cap, and the use of Si implant ions were key and unique features in establishing process repeatability. Simultaneously, improvements in the ohmic contact resistance have resulted in high performance FETs and TEDs, as well as integrated circuits with devices which have uniform electrical parameters. The medium scale integration level demonstrated with the ripple counter and the 49-stage ring oscillator, suggest that the analog multiplier is achievable with our present in-place process technology, during the next few months.

Two test chips are required for task 5 of Phase 1 of the program. The first test chip is designed for characterization of MESFETs, TEDs, thin-film and ion-implanted resistors, spiral inductors, and capacitors. A computer-generated plot of this test chip is shown in Figure 4-43. The overall chip size is 0.150 x 0.160 inch. The second test chip, containing a variety of analog multiplier circuits, has been designed and the photomask will be completed shortly. The wafer fabrication of both these test chips will commmence during April and May, respectively. The fabrication sequence established during the recent process development phase will be used to fabricate these devices and circuits.

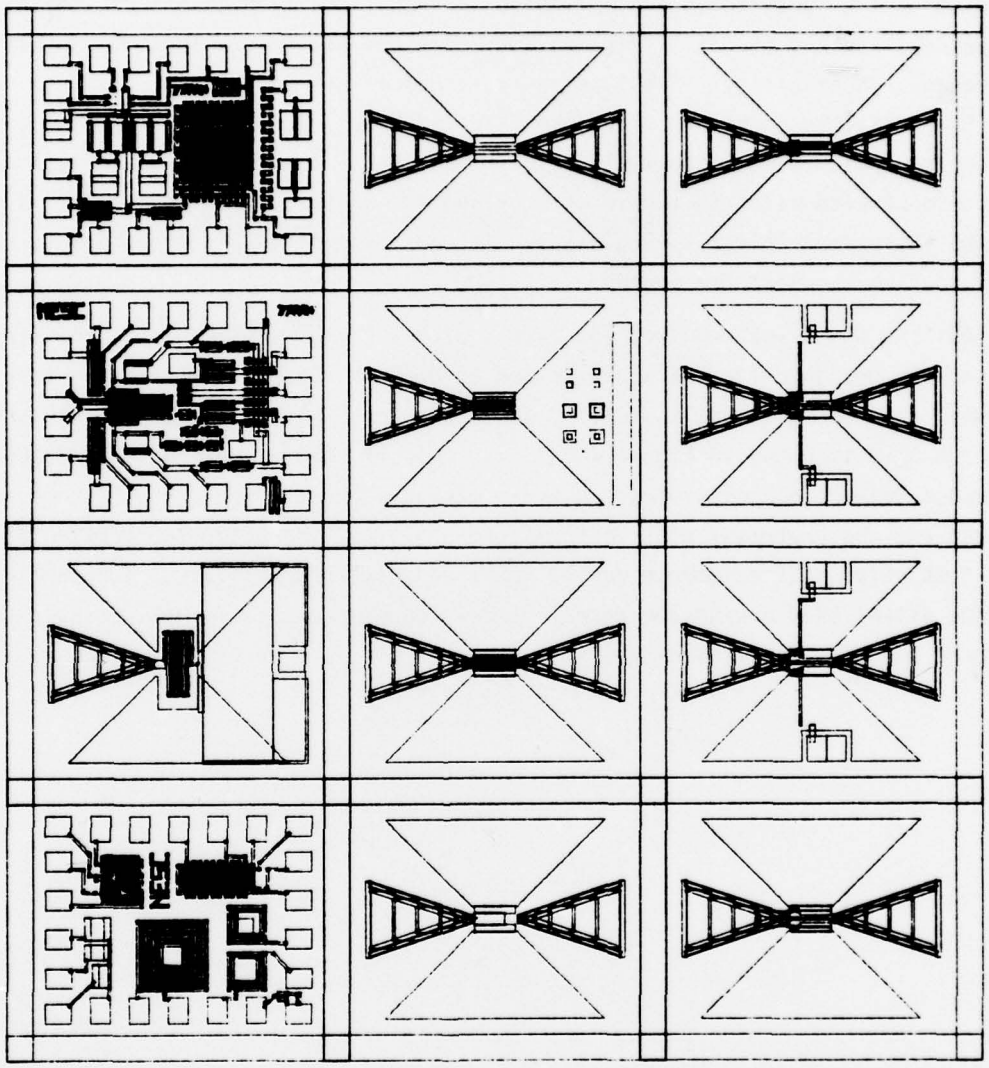


Figure 4-43. Computer Generated Plot of First Test Chip for Phase One

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5. CIRCUIT TECHNIQUES STUDY

The purpose of the circuit techniques study task was essentially to perform an initial design of each of the building block circuits to further detail the processing requirements, and to perform both theoretical and experimental studies of the alternatives for reactive components. This study was divided into three main subtasks:

- A generalized study of the building block circuits
- A study of the effects of process tolerances on circuit performance
- Detailed designs of the analog multipliers.

In performing this study, TRW was able to draw heavily on its silicon RF-LSI design experience to focus quickly on circuit approaches which lend themselves to monolithic implementation, and considerable attention was paid to minimization of active device count. For the process tolerance study, a recently completed amplifier design was used as a test case. This study showed that amplifier performance was most strongly dependent on inductor values and active layer thickness and only weakly dependent on doping concentration, capacitor values, and resistor values. While performing these first two study tasks, a thin film flat spiral inductor design procedure was developed and experimentally verified. Tests were also performed on a wide range of both inductors and capacitors to measure component Qs and parasitic capacitances. Finally, a detailed study of analog multiplier designs was carried out, starting with four basic alternatives, and settling on the two designs which are now being fabricated.

The following sections describe the results of each of the subtasks starting with the building block circuits.

5.1 BUILDING BLOCK CIRCUITS STUDY

The circuit design studies began with an examination of the RF characteristics of the FETs. The initial concept was to use small geometry devices (say 50 μm gate widths) to minimize dc power and chip area. However, the FET model soon showed two serious drawbacks with this approach. First, the input and output reflection coefficients (S_{11} and S_{22}) of these small geometry FETs had magnitudes between 0.95 and 0.99, and impractically large and high-Q reactive components would be required for impedance matching. Second, the devices had very large regions of potential instability, making parasitic oscillations within the circuits a strong possibility. This led to consideration of larger devices, and we have adopted the criteria that the magnitudes of both S_{11} and S_{22} must be less than 0.8 over the frequency range of interest. Additionally, the devices when embedded in their matching networks must be unconditionally stable from dc to 20 GHz. Instabilities above 20 GHz are virtually impossible in any reasonable circuit configuration. To satisfy these criteria, it was necessary to increase the device widths to 250 to 400 μm with the smaller devices used at higher frequencies.

Next, a simple cascade of two common source FETs driven by and driving 50 ohm lines was studied to determine the required range of reactive components for proper impedance matching. It was always possible to design this amplifier circuit for at least a 20% bandwidth with inductor values no larger than 20nH, and capacitors of less than 10pF from 2 to 12 GHz. A preliminary layout of this circuit showed that the initial concern about device size was somewhat misplaced, as the layout area tended to be dominated by the reactive components rather than the FETs. Further, the FETs can be biased such that the dc power is quite low without serious impact on the S-parameters. Section 5.2 shows a broadband high gain amplifier design which requires less than 150mW of dc power. The analog multiplier designs in Section 5.3 require only about 100mW, less than our best bipolar transistor designs which of course operate at much lower frequencies.

Having reached these fairly general design guides, preliminary designs for each of the building block circuits were studied. The conclusions of those studies are discussed next.

5.1.1 Amplifiers

Once the choice of basic topology is made, all FET amplifier designs proceed along similar lines. That is, one provides impedance transforming networks which match the output impedance of one device to the input impedance of the next device. FETs have a fairly large capacitive reactance associated with both input and output impedances, and so the transforming networks are invariably inductive, usually with at least one small series inductor and a larger shunt inductor. Additionally, since we prefer to avoid complicated dc level shifting schemes, a large value series capacitor is placed between devices. Biasing is provided through either the shunt inductors (drain) or through large shunt resistors (gate). See Section 5.2 for a detailed amplifier design example.

The basic topology choice for the monolithic amplifiers is between a balanced design and a single ended design. This choice was resolved in favor of the single ended approach because the device count, chip area, and dc power would all be lower by a factor of more than 2. The primary attraction of the balanced approach is that it can be driven through a hybrid and be presented with the optimum noise source impedance while the hybrid's input VSWR would be low. However, our studies showed that it would be possible to provide a good power transfer input impedance match (low VSWR) and still satisfy the 3dB noise figure goal for the X-band preamplifier in the single ended design.

The remaining amplifier design issue is the implementation of automatic gain control (AGC). Two good choices emerged for AGC. One is to use an analog multiplier, with one input the RF signal and the second input a dc amplitude control voltage

(see Section 5.3 for further explanation). The other choice is to place a variable load resistor in the drain circuit of one or more of the amplifying stages. The variable load resistor is nothing more than a FET operating in its linear region with the drain-to-source impedance serving as the variable load, and the gate voltage used for load control. Control of the bias of the amplifying device itself was studied but rejected because it changes the reactive component of the device's input impedance to the extent that the amplifier's frequency response is seriously compromised.

5.1.2 Oscillators

There are several oscillator types employed in microwave systems and thus of interest as building block circuits, including fixed tuned, narrow tuning, wide tuning, and oscillators with quadrature outputs. If there is to be any allowance made for process tolerances, all candidates for monolithic implementation must be voltage tuned, if only so they can be set to a specific frequency. For analysis purposes, all oscillators can be divided into either negative resistance oscillators or phase shift or feedback type oscillators. The phase shift oscillators would seem most attractive for our purposes, since all components can be implemented monolithically.

Phase shift oscillators basically consist of an amplifier and a feedback network. The oscillation frequency is the frequency at which the total pahse shift through the amplifier and feedback loop is an integer multiple of 2π, and the amplifier gain is equal to or greater than the loss in the feedback path. The desired phase shift is achieved in part through at least one active FET, say through a gate-source junction. Frequency tuning is accomplished by varying the bias on the FET in the feedback network, so that its phase shift changes and the loop equations are satisfied at some new frequency. In principle, this type of oscillator can be made to tune over a very wide range by using several FETs in the feedback loop. This design approach also lends itself to providing oscillators with quadrature outputs, but it turns out that these will not be required for the GaAs RF-LSI circuits as will be shown below.

A detailed design study of phase shift oscillator designs revealed two serious flaws which we have not been able to overcome. First, the phase shift through a FET is not only a function of bias, but is also a strong function of temperature. The SPICE analysis showed that as temperature was changed over a 50°C range, the frequency change due to temperature was actually larger than the frequency change due to tuning voltage. Second, the Qs of feedback networks containing active FETs were so low as to make poor phase noise performance a certainty. These two factors caused us to drop the phase shift oscillator approach and to turn to negative resistance designs.

Negative resistance oscillators satisfy the deceptively simple design equation

$$Z_d + Z_c = 0$$

or

$$R_d + jx_d + R_c + jx_c = 0$$

where the subscript d refers to the oscillating device and the subscript c refers to the tuning circuit. One general "problem" associated with FETs, particularly small ones, is that they are only conditionally stable. This means that it is possible to load the source and/or drain in such a way that the impedance seen looking in at the gate contains a negative real part. For example, if a small inductor is placed in series between the FET source and ground, there will be a wide frequency range over which the gate impedance will be -R(f) + jx(f). If a variable capacitance (a varactor) is placed between the FET gate and ground, the FET will oscillate at the frequency at which the magnitude of the varactor's reactance is equal to the magnitude of the FET's reactance. The oscillation frequency is changed by adjusting the varactor bias.

This design approach has the drawback that it requires an off-chip varactor, but has the overwhelming advantage that it works. The phase noise performance is dominated by the varactor Q and should be competitive with discrete component VCOs. The temperature stability is much better than it is for the phase shift design.

The proposed VCO design will consist of a FET with an inductor in its source circuit, a tuning varactor in its gate circuit, and a buffer amplifier in the drain circuit. The SPICE analysis showed that by selecting different varactors and by shorting out turns of the flat spiral inductor, a single FET could be made to operate from at least 2 to 12 GHz. The tuning range of a particular design will primarily be limited by the buffer amplifier bandwidth.

5.1.3 Modulators and Demodulators

Under a previous contract sponsored by the Office of Naval Research (N00014-76-C-0570), TRW had developed very high data rate (> 1.0 Gbps) BPSK modulator and demodulator circuits using GaAs IC technology. For the Phase III receiver function, a modulator circuit is required for spread spectrum despreading at the receiver front end. Between now and the first couple of months of Phase III a choice must be made between using the previous TED/FET modulator circuit for this function or using the analog multiplier circuit. That choice will be made during Phase II based on the comparative performance of the two circuits. At this point, however, it seems to us that the analog multiplier is the better candidate. The balanced configuration of the analog multiplier designs (see Section 5.3) should allow the adjustment of offset voltages to ensure at least 40 dB of carrier suppression, about 13 dB better than we have seen on the TED/FET modulator circuit.

The choice for the demodulator function is between a Costas loop design or the all-TED BPSK demodulator. The Costas demodulator requires three analog multipliers,

a VCO, two lowpass filters, and a loop filter. The TED circuit requires only three active devices. The choice is obvious.

5.1.4 Reactive Component Studies

After determining the range of reactive component values (inductors to 20 nH, capacitors to 10 pF), we decided that it would be prudent to fabricate and test these components, and in particular to measure their Qs. Capacitors of the metal-oxide-metal variety have been in use as part of the GaAs IC process for over 2 years, and required no new development. Flat spiral inductors have been used previously on 25 mil alumina substrates, but had not been fabricated with the small dimensions appropriate to monolithic ICs. There are several design methods available for these inductors, the most complete of which is called the "expanded Grover method."* This was reduced to a computer program which is listed below, and was used to design several different inductors. Several different series inductor-capacitor resonant circuits were fabricated on GaAs substrates and characterized on the network analyzer. This sort of characterization allows one to easily determine the inductor and capacitor values and associated Qs. The capacitors typically vary ± 10% from their design values, apparently due to variations in the oxide thickness. The Qs associated with the capacitors are about 10 at 10 GHz. The inductors matched their design values very accurately:

Calculated Inductance (nH)	Measured Inductance (nH)
2.74	2.70
4.60	4.60
9.43	9.90

The differences are typically less than the measurement accuracy of the test equipment.

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* H.M. Greenhouse, "Design of Planar Rectangular Microelectronics Inductors," IEEE Trans., Volume PHP-10, No. 2, June 1974.

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100   PRINT"THIS PROGRAM CALCULATES THE INDUCTANCE OF A PLANAR"
110   PRINT"RECTANGULAR MICROELECTRONICS COIL. ALL DIMENSIONS"
120   PRINT"MUST BE GIVEN IN CMS. OPERATING FREQUENCY MUST BE"
130   PRINT"GIVEN IN GHZ. S=INTER-TRACK SPACING. W=TRACK WIDTH"
140   PRINT"T=SEGMENT THICKNESS. RO=METAL RESISTIVITY (OHMS-CM)."
150   PRINT"L1,L2=LENGTHS OF OUTER SEGMENTS. N=NUMBER OF TURNS."
160   PRINT"ENTER S,W,T,L1,L2,N,F,RO"
170   INPUT S,W,T,L1,L2,NO,FO,RO
180   PRINT"S(CMS)=";S;"  W(CMS)=";W;"  T(CMS)=";T
190   PRINT"L1(CMS)=";L1;"  L2(CMS)=";L2;"  N=";NO;"  F(GHZ)=";FO
200   Z=4*NO
210   N=FIX(NO)
220   EO=FIX(Z/2)
230   DO=Z-EO
240   DIM L(Z)
250   DIM G(Z-2,Z)
260   DIM A(Z-2,Z)
270   DIM A$(Z-2,Z)
280   DIM P(Z-2,Z)
290   DIM Q(Z-2,Z)
300   DIM M(Z-2,Z)
310   DIM B(Z-2,Z)
320   DIM C(Z-2,Z)
330   DIM D(Z-2,Z)
340   DIM E(Z-2,Z)
350   DIM F(Z-2,Z)
360   DIM H(Z-2,Z)
370   DIM B$(Z-2,Z)
380   DIM C$(Z-2,Z)
390   DIM D$(Z-2,Z)
400   DIM E$(Z-2,Z)
410   DIM F$(Z-2,Z)
420   DIM H$(Z-2,Z)
430   L(1)=L1
440   L(2)=L2
450   L3=0
460   L4=0
470   S1=2*L1*(LOG(2*L1/(W+T))+0.50049+(W+T)/(3*L1))
480   S2=2*L2*(LOG(2*L2/(W+T))+0.50049+(W+T)/(3*L2))
490   FOR Y1=2 TO Z STEP 1
500   IF Y1>EO THEN 530
510   L(2*Y1)=L2-(Y1-1)*(W+S)
```

```
520   IF L(2*Y1)>0 THEN 560
530   PRINT"DIMENSION L2 INCOMPATIBLE WITH NUMBER OF TURNS,"
540   PRINT"INCREASE IN L2 OR REDUCTION OF TURNS SUGGESTED."
550   GOTO 160
560   L4=L4+L(2*Y1)
570   S2=S2+2*L(2*Y1)*(LOG(2*L(2*Y1)/(W+T))+0.50049+(W+T)/(3*L(2*Y1)))
580   IF Y1>DO THEN 570
590   L(2*Y1-1)=L1-(Y1-2)*(W+S)
500   IF L(2*Y1-1)>0 THEN 640
510   PRINT"DIMENSION L1 INCOMPATIBLE WITH NUMBER OF TURNS,"
520   PRINT"INCREASE IN L1 OR REDUCTION OF TURNS SUGGESTED."
530   GOTO 160
540   L3=L3+L(2*Y1-1)
550   S1=S1+2*L(2*Y1-1)*(LOG(2*L(2*Y1-1)/(W+T))+0.50049+(W+T)/(3*L(2*Y1-1)))
560   NEXT Y1
570   LO=S1+S2
580   L5=L3+L4+L2+L1
590   PRINT "RO(OHMS)=";RO;"   TOTAL LENGTH OF SEGMENTS (CM)=";L5
700   REM  CALCULATION OF MUTUAL INDUCTANCE TERMS
710   X=1
720   E1=4*N*(N-1)+2*N*(Z-4*N)
730   YO=Z-4
740   GOTO 770
750   E1=4*N^2+2*N*(Z-4*N)+(Z-4*N-2)*(Z-4*N-1)*(Z-4*N)/3
760   YO=Z-2
770   K=0
780   IO=0
790   FOR J=1 TO N STEP 1
800   FOR Y=1 TO YO STEP 1
810   IF X=0 THEN 840
820   K1=Y+4*J
830   GOTO 850
840   K1=Y+4*J-2
850   IF K1>7  THEN 1270
860   K=K+1
870   IF K>E1 THEN 1280
880   IF X=0 THEN 910
890   AO=J*(W+S)
900   GOTO 920
910   AO=L(K1-1)+(J-1)*(S+W)
920   A1=AO/W
930   A(Y,K1)=LOG(AO)-1/12/A1^2-1/60/A1^4
```

```
940   A$(Y,K1)=1/158/A1↑5+1/360/A1↑9+1/660/A1↑13
950   G(Y,<1)=EXP(A(Y,K1)-A$(Y,K1))
960   IF X=0 THEN 990
970   Q(Y,K1)=J*(W+S)
980   GOTO 1000
990   Q(Y,K1)=(J-1)*(W+S)
1000   IF Y=1 THEN 1030
1010   P(Y,K1)=J*(W+S)
1020   GOTO 1040
1030   P(Y,K1)=(J-1)*(W+S)
1040   B(Y,K1)=G(Y,<1)/(L(K1)+P(Y,K1))-SQR(1+(G(Y,K1)/(L(K1)+P(Y,K1)))↑2)
1050   C(Y,K1)=LOG((L(K1)+P(Y,K1))/G(Y,K1)+SQR(1+((L(K1)+P(Y,K1))/G(Y,K1))↑2))
1060   D(Y,K1)=2*(L(<1)+P(Y,K1))*(B(Y,<1)+C(Y,K1))
1070   E(Y,K1)=G(Y,K1)/(L(<1)+Q(Y,K1))-SQR(1+(G(Y,K1)/(L(K1)+P(Y,K1)))↑2)
1080   F(Y,K1)=LOG((L(K1)+Q(Y,K1))/G(Y,<1)+SQR(1+((L(K1)+Q(Y,K1))/G(Y,K1))↑2))
1090   H(Y,K1)=2*(L(<1)+Q(Y,K1))*(E(Y,<1)+F(Y,K1))
1100   IF P(Y,K1)=0 THEN 1120
1110   GOTO 1140
1120   B$(Y,K1)=0
1130    GOTO 1150
1140   B$(Y,K1)=G(Y,<1)/P(Y,K1)-SQR(1+(G(Y,<1)/P(Y,K1))↑2)
1150   C$(Y,K1)=LOG(P(Y,<1)/G(Y,K1)+SQR(1+(P(Y,<1)/G(Y,K1))↑2))
1160   D$(Y,K1)=2*P(Y,K1)*(B$(Y,K1)+C$(Y,<1))
1170   IF Q(Y,K1)=0 THEN 1190
1180   GOTO 1210
1190   E$(Y,K1)=0
1200   GOTO 1220
1210   E$(Y,K1)=G(Y,<1)/Q(Y,K1)-SQR(1+(G(Y,<1)/Q(Y,K1))↑2)
1220   F$(Y,K1)=LOG(Q(Y,<1)/G(Y,K1)+SQR(1+(Q(Y,<1)/G(Y,K1))↑2))
1230   H$(Y,K1)=2*Q(Y,K1)*(E$(Y,<1)+F$(Y,K1))
1240   M(Y,K1)=D(Y,K1)+H(Y,<1)-D$(Y,<1)-H$(Y,<1)
1250  ID=ID+M(Y,K1)
1260  NEXT Y
1270  NEXT J
1280 IF X=0 THEN 1320
1290  M1=ID
1300  X=0
1310  GOTO 750
1320  M2=ID
1330  R=RO*L5/W/T
1340  QQ=2*PI*FO*(LO+M1-M2)/R
1350  PRINT"LO=";LO;"   M(+)=";M1;"   M(-)=";M2;"  R(OHMS)=";R
```

```
1360  PRINT"L(NH)=";LO+M1-M2;"    Q AT";FO;"GHZ=";QO
1370  PRINT
1380  PRINT"DO YOU WISH CALCULATION OF PARASITICS? (1 OR 0)";
1390  INPUT XO
1400  IF XO=0 THEN 1480
1410  E2=8.854E-14
1420  E3=12.5
1430  PRINT"ENTER COIL TO GROUND PLANE SEPARATION (CMS)";
1440  INPUT DO
1450  C1=E3*E2*W*L5/DO
1460  PRINT"COIL TO GROUND PLANE SEPARATION (CMS)=";DO
1470  PRINT"PARASITIC CAPACITANCE TO GROUND FOR GA.AS.(PF)=";C1*1E12
1480  END
```

5.2 ONR PREAMPLIFIER DESIGN

Concurrent with the general circuit design studies described above, a very specific design example was being carried out on another program. Since this design example made use of both the FET model and COMPACT, and the results provide specific illustrations of the points made above, the results are summarized here.

The circuit design goals for the monolithic preamplifier being developed the Office of Naval Research (Contract N00014-77-0645) can be summarized as follows:

Gain	30 dB
Bandwidth	8 to 11 GHz
Noise figure	<3.0 dB
DC power consumption	<500 mW

TRW has performed the theoretical design of the low noise preamplifier with the following predicted performance.

Gain	30.16 dB at 10 GHz
Bandwidth	8 to 11 GHz
Noise figure	2.95 dB at 10 GHz
DC power consumption	150 mW

In order to meet the low noise figure requirements, extensive use was made of the computer model for microwave FETs described in Section 2 and Appendices A and B.

The chosen device has the following characteristics (nominal)

L_g = 1 μm	Gate length
d = 0.34 μm	Channel depth
$n_o = 3.5 \times 10^{16}$	Carrier doping density in the channel
Z = 360 μm	Device width
L_{SG}, L_{GD} = 1.0 μm	Source-gate, gate-drain separation
$n \geq 1 \times 10^{17}$ cm^{-3}	Carrier doping density underneath the contact areas (source and drain)

This device under the biasing conditions $V_{DS} \simeq 3.0$ volts, $V_{gs} \simeq -2.0$ volts. $I_{DS} \simeq 5.2$ mA has the following predicted S parameters:

F(GHz)	S_{11}	S_{21}	S_{12}	S_{22}
8	0.79 /-60.0	1.199 /118.7	0.159 /44.9	0.862 /-32.8
9	0.758 /-65.5	1.138 /113.0	0.169 /41.2	0.848 /-35.9
10	0.739 /-70.5	1.079 /107.7	0.177 /37.8	0.835 /-38.8
11	0.701 /-79.4	1.025 /102.8	0.184 /34.7	0.824 /-41.5

The predicted noise figure of the device under optimum source impedance is 2 dB at 10 GHz.

The gate length of 1 μm was selected as the longest length (higher yield) consistent with the gain, frequency response, and noise figure goals. The gate width of 360 μm was selected because it reduces the magnitude of S_{11} and S_{22} to levels which can practically be matched by monolithic passive devices, and to help ensure unconditional stability of the amplifier.

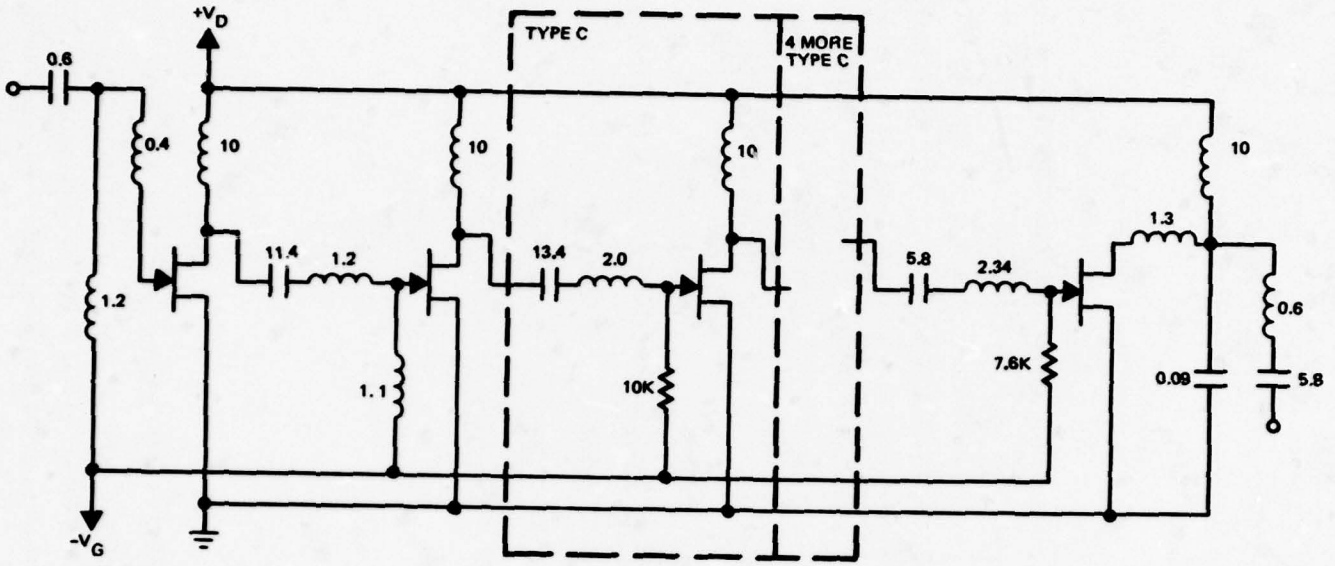
In order to meet the 30 dB gain requirement, eight stages of amplification are used in the design. The interstage matching network between stages 1 and 2 as well as the input network to stage 1 were synthesized with reactive elements only in order to avoid noise contributions from resistive sources. These networks also present the corresponding optimum source impedance to the FET devices of stages 1 and 2. The overall schematic of the low noise preamplifier is shown in Figure 5-1. Stages 1 and 2 are followed by five amplification stages with an overall gain of approximately 20 dB. The output stage provides approximately 4 dB of gain and has an output matching network that couples into a 50 ohm load.

The predicted S-parameters and noise figure of the amplifier are:

F(GHz)	S_{11}	S_{21}	S_{12}	S_{22}
8	0.40 /-78	33.39 / -70.9	0.000 / 58.7	0.42 / -50
9	0.23 /-88	30.04 /-164.6	0.000 / -19.0	0.27 / -67
10	0.22 /-65	32.20 / 90.8	0.000 /-108.4	0.06 /-102
11	0.41 /-73	31.46 / -46.6	0.000 / 128.6	0.19 / 70

	Gain (dB)	NF (dB)
8	30.47	3.16
9	29.55	2.98
10	30.16	2.95
11	29.95	3.04

The preceding has been a very brief description of the amplifier design process. The point that we wish to illustrate here is not the amplifier design itself, but the use of the process related FET model and COMPACT for design evaluation. Specifically, both models were exercised to determine the amplifiers performance dependence on process control tolerances. The only assumption is that the process variations would be systematic rather than random. That is, if a particular resistor value was 10% higher than the design value, all resistors would be 10% high. This is almost universally typical of monolithic IC fabrication.



ALL CAPACITOR VALUES IN pF
ALL INDUCTOR VALUES IN nH
ALL RESISTOR VALUES IN OHMS
$V_D \simeq 3.0$ VOLTS
$V_G \simeq -2.0$ VOLTS
$I_{DS} \simeq 5.2$ mA

FET CHARACTERISTICS (NOMINAL)
$L_g = 1.0 \mu m$
$d = 0.34 \mu m$
$n_o = 3.8 \times 10^{16}$ (IN CHANNEL)
$Z = 360 \mu m$
$n \geq 1 \times 10^{17}$ (CONTACT AREAS)
$L_{SG}, L_{GD} = 1.0 \mu m$

Figure 5-1. Preamplifier Schematic

Figure 5-2 shows the amplifier performance with all components at their nominal values. Figures 5-3 through 5-7 show performance variations as a function of channel depth (Figure 5-3), doping concentration (Figure 5-4), resistor values (Figure 5-5), capacitor values (Figure 5-6), and inductor values (Figure 5-7). In each case the values were increased and decreased by 10% from the nominal values. The bais voltages were readjusted after each change to try to minimize the impact of the change.

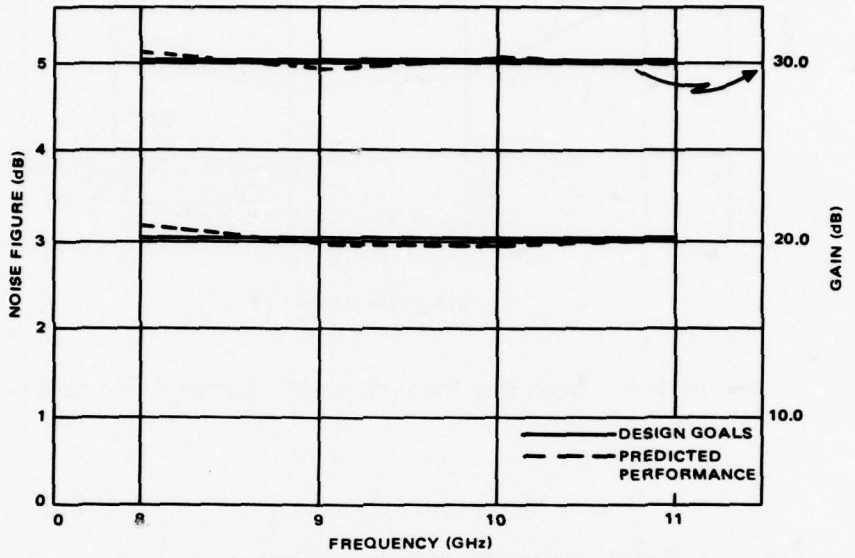


Figure 5-2. Amplifier Performance

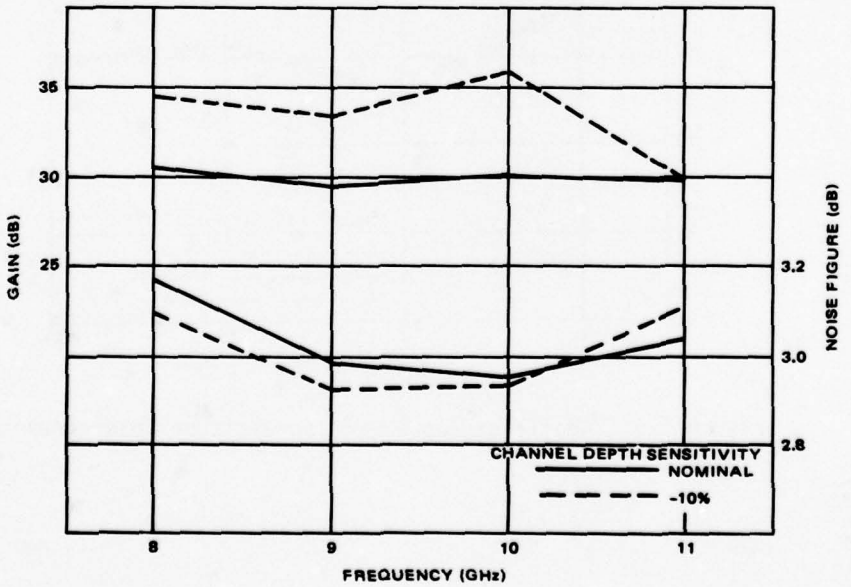


Figure 5-3. Amplifier Variation with Channel Depth

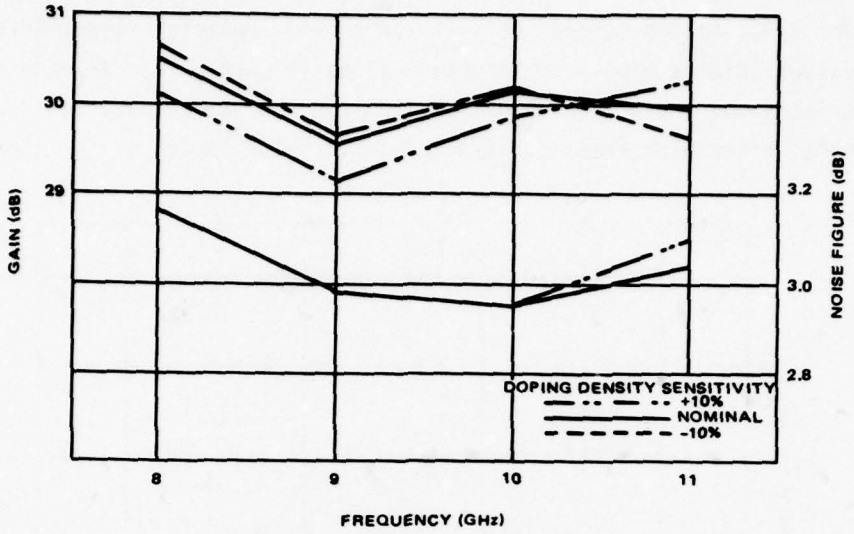


Figure 5-4. Amplifier Variation with Doping Concentration

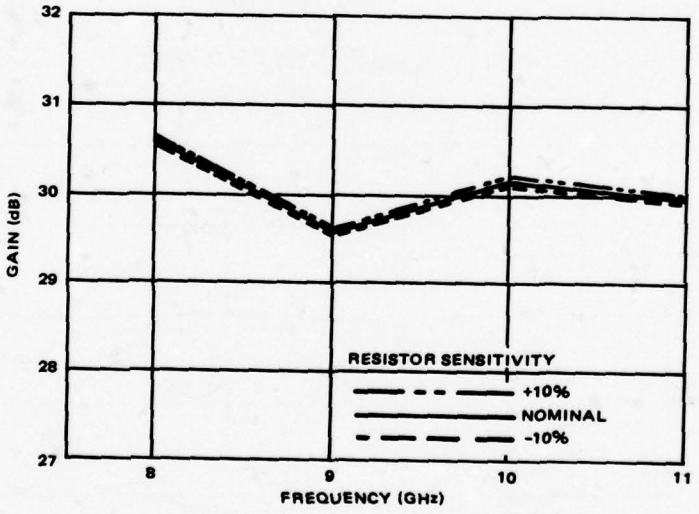


Figure 5-5. Amplifier Dependence on Resistor Tolerances

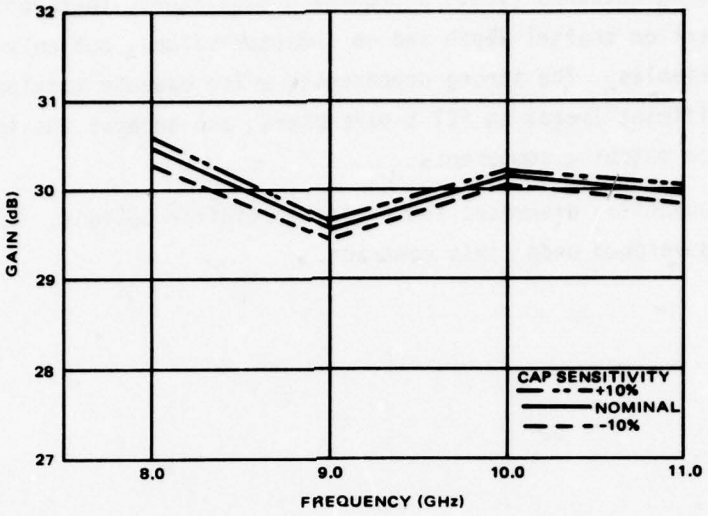


Figure 5-6. Amplifier Performance Variation with Capacitor Tolerances

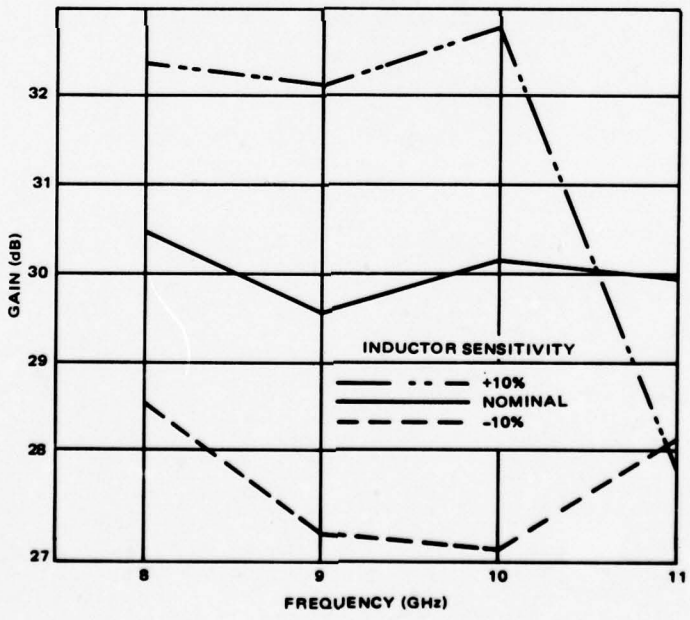


Figure 5-7. Amplifier Performance Dependence on Inductor Values

One can conclude from the figures that, at least for an amplifier with tuned interstage matching networks (i.e., a broadband amplifier), that performance will be strongly dependent on channel depth and on inductor values, but only weakly dependent on the other variables. The strong dependences arise because varying channel thickness has a significant impact on FET S-parameters, and because the inductors are the primary impedance matching components.

The next subsection discusses the analog multiplier designs. These are the first circuits to be developed under this contract.

5.3 ANALOG MULTIPLIER

Analysis of the various alternatives for analog multiplier circuits requires both a small signal and large signal device model for reasons which will become apparent shortly. While TRW's FET computer model does provide both small signal and large signal outputs, the form of the large signal output is more complicated than needed for comparative analysis of the multiplier designs. Therefore, we here develop simplified expressions for FET large signal characteristics.

First, consider a FET biased into current saturation. If the average depletion depth under the gate is called χ, the drain current can be approximated by

$$I_{ds} = I_{dss}\left(1 - \frac{\chi}{a}\right) \tag{5.1}$$

where I_{dss} is the value of I_{ds} associated with χ equal to zero, and "a" is the active layer thickness. While this expression does not properly account for resistive drops outside the gate, there are typically two or more orders of magnitude less than the resistive drop under the gate. The common expression for depletion depth is

$$\chi = \left[\frac{2\,\varepsilon_r\,\varepsilon_o}{nq}\,(V + \phi)\right]^{1/2} \tag{5.2}$$

where

V = applied potential

ϕ = built in potential

n = doping concentration

q = electronic charge

ε_r = relative dielectric constant

ε_o = dielectric constant of free space

By the definition of pinch off voltage, V_p, we can write

$$a = \left[\frac{2\,\varepsilon_r\,\varepsilon_o}{nq}\left(V_p + \phi\right)\right]^{1/2} \tag{5.3}$$

This gives

$$\frac{\chi}{a} = \left(\frac{V + \phi}{V_p + \phi}\right)^{1/2} \tag{5.4}$$

If we absorb the built in potential into our definition of the applied voltages, equation (5.1) can be rewritten as

$$I_{DS} = I_{DSS}\left[1 - \left(\frac{V_{gs}}{V_p}\right)^{1/2}\right] \tag{5.5}$$

equation (5.5) is of the general form $f(\chi) = 1 - \sqrt{\chi}$, which, for $0 \leq \chi \leq 1$ can be closely approximated by

$$f(\chi) \simeq (1 - \chi)^2 \qquad 0 \leq \chi \leq 1 \tag{5.6}$$

The two functions are plotted in Figure 5-8 to show their approximate equality. Substituting the form of equation (5.6) into equation 5.5) gives

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tag{5.7}$$

While it may seem that several assumptions have been accumulated which render equation (5.7) of doubtful accuracy, it is clearly possible to exactly describe the relationship between I_{DS}, V_{gs}, and V_p in terms of a binomial series of the form

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^N \tag{5.8}$$

While this is mathematically correct, it doesn't offer much physical insight. The preceding was an attempt to lend physical insight while arriving at an expression useful for multiplier analysis. It will be shown below that best analog multiplier performance is obtained when the exponent N = 2. It will be further shown by device measurement data that N = 2 is a very good estimate for devices fabricated on a uniform epi layer for gate lengths as short as 0.5 microns.

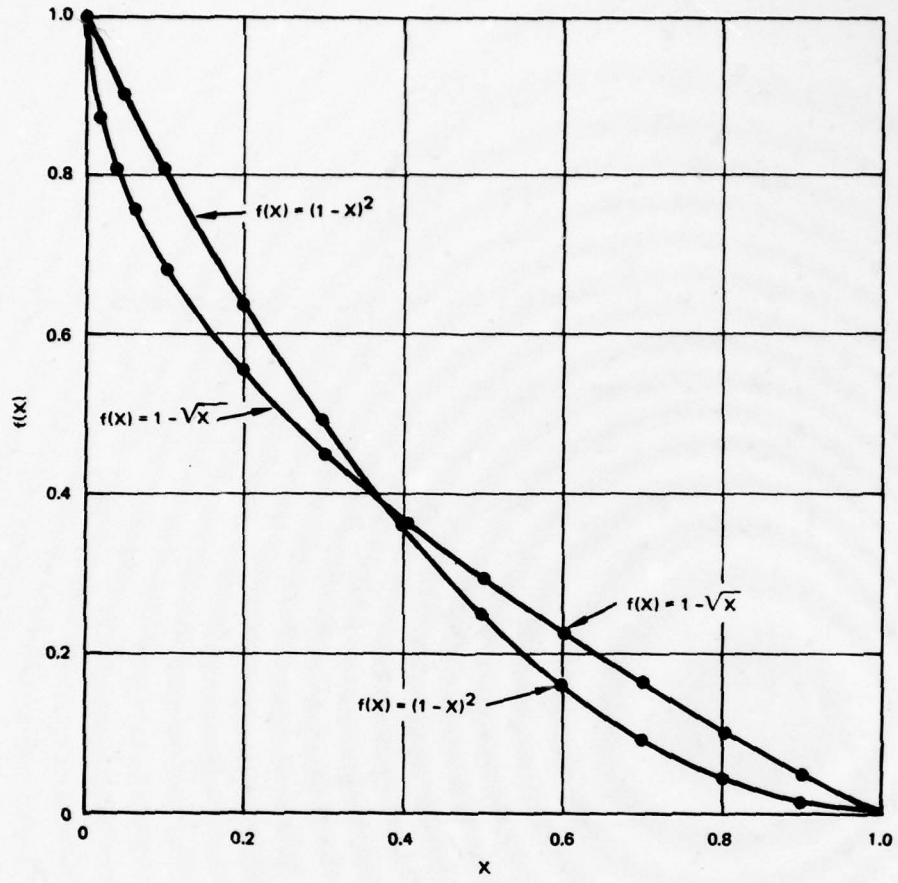


Figure 5-8. Comparison of $(1 - \sqrt{x})$ and $(1 - x)^2$

From (5.8), the FET transconductance is derived by differentiation of I_{DS} with respect to V_{gs}

$$g_m = - \frac{N I_{dss}}{V_p} \left(1 - \frac{V_{gs}}{V_p} \right)^{N-1} \qquad (5.9)$$

This expression shows that for N = 2 there will be a strong first order dependence of transconductance on V_{gs}, a device characteristic which is undesirable for wide dynamic range linear amplifier applications. Device manufacturers, like NEC for example, often seek out doping profiles which will result in N ≃ 1 and no transconductance dependence on V_{gs}. To reiterate, for analog multiplier design N = 2 is

optimum, while for amplifiers, N = 1 is optimum. The value of N for a particular device is readily determined from standard I-V measurements and by observing from (5.8) that

$$N = \frac{\log\left(\frac{I_{ds}}{I_{dss}}\right)}{\log\left(1 - \frac{V_{gs}}{V_p}\right)} \tag{5.10}$$

Next, we are interested in modeling the resistance (or conductance) of the FET in the linear region. Let

R_{sg} = resistance from source to gate

R_g = resistance in the gate area

R_{gd} = resistance from gate to drain

$$R_{total} = R_{sg} + R_g + R_{gd} = \frac{l_{sg} + l_{gd}}{nq\ \mu a\ Z} + \frac{l_g}{nq\ \mu a\ Z}\ \frac{1}{\left(1 - \frac{V_{gs}}{V_p}\right)^2} \tag{5.11}$$

$$R_{total} = nq\ \mu a\ z \left[l_{sg} + l_{gd} + \frac{1}{\left(1 - \frac{V_{gs}}{V_p}\right)^2} \right] \tag{5.12}$$

It will be seen below that the FETs which are to be biased into their linear region are best used near their minimum resistance to maximize the analog multipliers transfer gain. A typical bias point might be such that $V_{gs} \simeq 0.3\ V_p$. At this quiescent bias the conductance of the FET in the linear region is often experimentally found to be close to the transconductance of the same device under the same bias conditions. After supporting this claim with experimental data below, we will let

$$g_{DS}\ (\text{linear region}) \simeq g_m = -\frac{N\ I_{dss}}{V_p}\left(1 - \frac{V_{gs}}{V_p}\right)^{N-1} \tag{5.13}$$

$$= -\frac{2\ I_{dss}}{V_p}\left(1 - \frac{V_{gs}}{V_p}\right) \text{ for } N = 2$$

The following data verifies that our reasonably simple dc FET models have credibility.

Several FETs were examined and experimental results show that the DXL2503 half micron FETs very closely obey this simple model. Shown in Figures 5-9 and 5-10 are the measured DC curves for two devices. The data used to generate the characteristics is given in Tables 5-1 and 5-2.

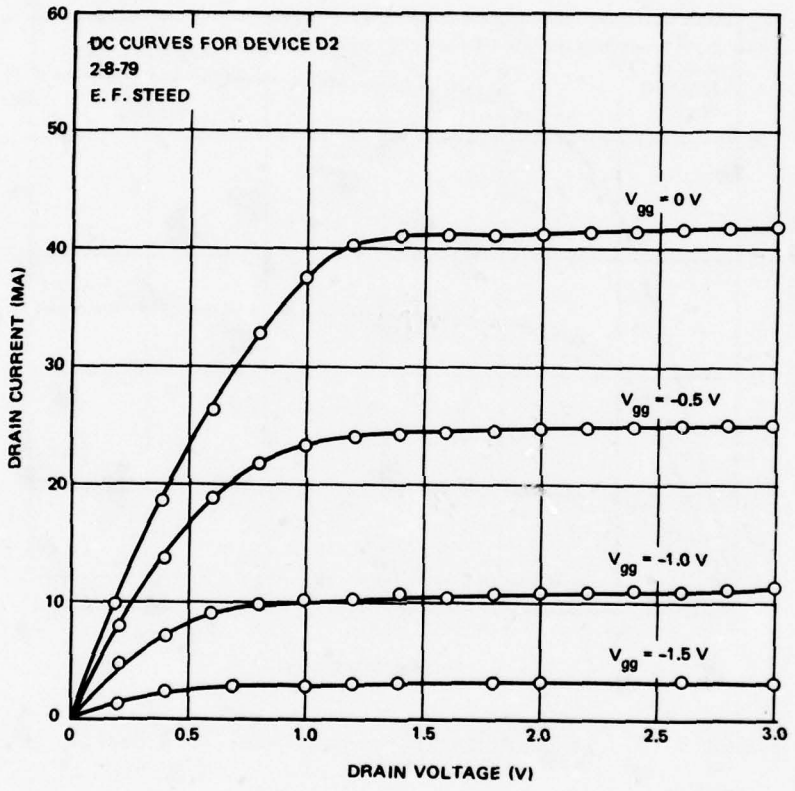


Figure 5-9. IV Characteristics of Dexcel 2503 Device D2

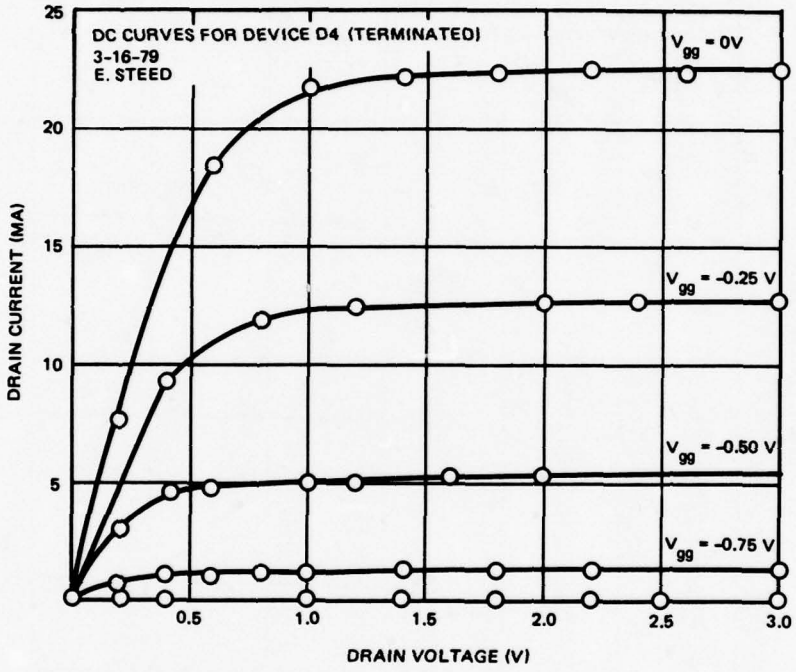


Figure 5-10. IV Characteristics of Dexcel 2503 Device D4

Table 5-1. Tabulated Data for DC Curves on Dexcel Device (D4)

V_{gs}	V_d	I_d	V_{gs}	V_d	I_d
			-0.5	0.2	3.05
0	0	0	-0.5	0.4	4.24
0	0.2	7.53	-0.5	0.6	4.63
0			-0.5	0.8	4.8
0	0.6	18.28	-0.5	1.0	4.9
0	1.0	21.76	-0.5	1.2	4.97
0	1.4	22.24	-0.5	1.4	5.04
0	1.8	22.37	-0.5	1.6	5.08
0	2.2	22.46	-0.5	1.8	5.13
0	2.6	22.46	-0.5	2.0	5.18
0	3.0	22.48	-0.5	2.2	5.21
			-0.5	2.4	5.25
-0.25	0	0	-0.5	2.8	5.34
-0.25	0.4	9.28	-0.5	3.0	5.36
-0.25	0.8	11.95			
-0.25	1.2	12.28	-0.75	0	0
-0.25	1.6	12.49	-0.75	0.2	0.75
-0.25	2.0	12.63	-0.75	0.4	0.92
-0.25	2.4	12.73	-0.75	0.6	1.0
-0.25	3.0	12.88	-0.75	0.8	1.04
			-0.75	1.0	1.08
-0.3	0	0	-0.75	1.4	1.12
-0.3	0.2	5.02	-0.75	1.8	1.16
-0.3	0.4	8.1	-0.75	2.2	1.20
-0.3	0.6	9.45	-0.75	3.0	1.26
-0.3	0.8	9.95			
-0.3	1.0	10.1	-1.00	0	0
-0.3	1.2	10.27	-1.00	0.4	0
-0.3	1.4	10.36	-1.00	0.6	0
-0.3	1.6	10.41	-1.00	0.8	0
-0.3	2.0	10.5	-1.00	1.0	0
-0.3	2.4	10.6	-1.00	1.2	0
-0.3	2.8	10.7	-1.00	1.4	0
-0.3	3.0	10.8	-1.00	1.6	0
			-1.00	2.0	0
			-1.00	2.4	0
			-1.00	2.8	0
			-1.00	3.0	0

Table 5-2. Tabulated Data for DC Curves on Dexcel Device (D2)

V_{gs}	V_d	I_d	V_{gs}	V_d	I_d
0	0	0	-1.0	0	0
0	0.2	9.7	-1.0	0.2	4.48
0	0.4	18.5	-1.0	0.4	7.15
0	0.6	26.1	-1.0	0.6	8.75
0	0.8	32.7	-1.0	0.8	9.77
0	1.0	37.5	-1.0	1.0	10.2
0	1.2	40.0	-1.0	1.2	10.3
0	1.4	40.9	-1.0	1.4	10.5
0	1.6	41.1	-1.0	1.6	10.5
0	1.8	41.1	-1.0	1.8	10.6
0	2.0	41.2	-1.0	2.0	10.7
0	2.2	41.2	-1.0	2.2	10.8
0	2.4	41.4	-1.0	2.4	10.9
0	2.6	41.5	-1.0	2.6	11.0
0	2.8	41.8	-1.0	2.8	11.1
0	3.0	42.2	-1.0	3.0	11.3
-0.5	0	0	-1.5	0	0
-0.5	0.2	7.8	-1.5	0.2	1.31
-0.5	0.4	13.9	-1.5	0.4	2.16
-0.5	0.6	18.7	-1.5	0.6	2.80
-0.5	0.8	21.8	-1.5	0.8	3.01
-0.5	1.0	23.3	-1.5	1.0	3.12
-0.5	1.2	24.0	-1.5	1.2	3.16
-0.5	1.4	24.1	-1.5	1.4	3.21
-0.5	1.6	24.4	-1.5	1.6	3.25
-0.5	1.8	24.4	-1.5	1.8	3.29
-0.5	2.0	24.6	-1.5	2.0	3.33
-0.5	2.2	24.7	-1.5	2.2	3.38
-0.5	2.4	24.8	-1.5	2.4	3.44
-0.5	2.6	25.0	-1.5	2.6	3.50
-0.5	2.8	25.2	-1.5	2.8	3.56
			-1.5	3.0	3.64

The data for device D2 follows a relationship given by the formula

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^N$$

where the exponent N is to be determined. Upon dividing and taking logs, N is given by

$$N = \frac{\log \frac{I_{ds}}{I_{dss}}}{\log\left(1 - \frac{V_{gs}}{V_p}\right)}$$

The following gives the calculated value of N:

N	I_{ds}	I_{dss}	V_{gs}	V_p
1.88	24.8	41.5	-0.5	-2.1
2.069	10.9	41.5	-1.0	-2.1
1.988	3.44	41.5	-1.5	-2.1

The average value of N is 1.98. This value is very close to an exponent of 2. Thus, in saturation the drain current of device D2 is accurately given by

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2$$

The drain conductance in the linear region is given by the formula

$$g_{ds} = \frac{-2I_{dss}}{V_p}\left(1 - \frac{V_{gs}}{V_p}\right)$$

Table 5-3 shows that the drain conductance in the linear region given by the above formula is accurate enough to predict the current in the voltage variable conductance.

Table 5-3. Device D2

V_d	V_g	Measured I_{ds}	Calculated $I_{ds} = \frac{-2I_{dss}}{V_p}\left(1 - \frac{V_{gs}}{V_p}\right) V_d$
.2	0	9.7	8.0
.4	0	18.5	16
.6	0	26.1	24
.8	0	32.7	31.62
.2	.5	7.8	6.4
.4	1.5	13.9	12.80
.6	.5	18.7	19.21
.2	-1	4.48	4.14
.4	-1	7.15	8.28
.2	-1.5	1.31	2.2

Similar calculations were performed on device D4 as shown in Table 5-4. The average value of N is 2.09, and for device D4 the drain current in the saturated region is

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2$$

Table 5-4. Device D4

N	I_{ds}	I_{dss}	V_{gs}	V_p
1.995	12.63	22.42	.25	1.0
2.127	10.5	22.42	.3	1.0
2.114	5.18	22.42	.5	1.0
2.124	1.18	22.42	.75	1.0

In subsequent analysis of the variable transconductance multiplier, dc data used in calculations will be data from the Dexcel DXL2503s. We expect similar large signal performance from our devices.

5.3.1 Analysis of Analog Multiplier Design No. 1

All six transistors in Figure 5-11 are biased in their saturation region. It is assumed that the transconductance is a function of gate voltage for these devices.

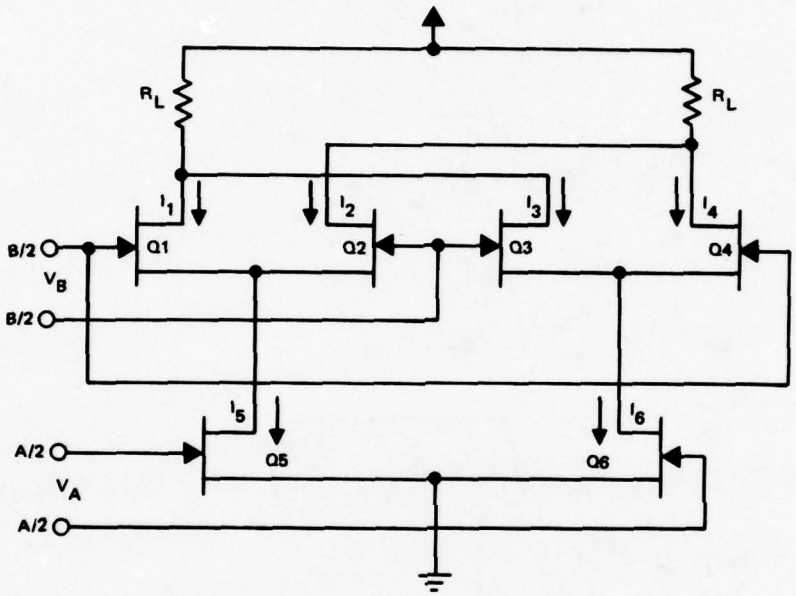


Figure 5-11. Transconductance Multiplier Schematic

It has been shown that, in general, for a square law device

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tag{5.14}$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{-2I_{dss}}{V_p}\left(1 - \frac{V_{gs}}{V_p}\right) = g_{mo}\left(1 - \frac{V_{gs}}{V_p}\right) \tag{5.15}$$

We will now show that the transconductance of the upper stage FET's Q1, Q2, Q3, Q4 is a function of the voltages applied to Q5 and Q6. g_m can be written as a function of I_{ds} by substituting (5.14) into (5.15)

$$g_m = \frac{-2I_{dss}}{V_p}\sqrt{\frac{I_{ds}}{I_{dss}}} = g_{mo}\sqrt{\frac{I_{ds}}{I_{dss}}} \tag{5.16}$$

$$I_5 = I_{dss}\left(1 - \frac{A/2}{V_p}\right)^2 \tag{5.17}$$

$$I_6 = I_{dss}\left(1 - \frac{\overline{A}/2}{V_p}\right)^2 \tag{5.18}$$

$$g_{m_{12}} = g_{mo}\sqrt{\frac{I_{ds1}}{I_{dss1}}}$$

$$g_{m_{12}} = g_{mo}\sqrt{\frac{\frac{1}{2}I_5}{I_{dss1}}}$$

$$g_{m_{12}} = g_m\sqrt{\frac{\frac{1}{2}I_{dss5}}{I_{dss1}}\left(1 - \frac{A/2}{V_p}\right)^2} \quad \text{but } \frac{1}{2}I_{dss5} = I_{dss1}$$

$$g_{m_{12}} = g_{mo}\left(1 - \frac{A/2}{V_p}\right) \tag{5.19}$$

$$g_{m_{34}} = g_{mo}\sqrt{\frac{I_{ds3}}{I_{dss3}}} = g_{mo}\sqrt{\frac{\frac{1}{2}I_6}{I_{dss3}}}$$

$$g_{m_{34}} = g_{mo}\sqrt{\frac{\frac{1}{2}I_{dss6}}{I_{dss3}}\left(1 - \frac{\overline{A}/2}{V_p}\right)^2}$$

$$g_{m\ 34} = g_{mo}\left(1 - \frac{\overline{A}/2}{V_p}\right) \tag{5.20}$$

This establishes that the upper stage transconductances are functions of the voltages applied to the lower stage FET's. The output voltage, V_o, is given by

$$V_o = R_L \left[g_{m\ 12}\ B + g_{m\ 34}\ \overline{B} \right]$$

But $B = -\overline{B}$

$$V_o = R_L\ B \left[g_{m\ 12} - g_{m\ 34} \right] \tag{5.21}$$

Substituting (5.19) and (5.20) into (5.21)

$$V_o = R_L\ B\ g_{mo} \left[\left(1 - \frac{A/2}{V_p} \right) - \left(1 - \frac{\overline{A}/2}{V_p} \right) \right]$$

$$= R_L\ B\ g_{mo} \left[- \frac{A/2}{V_p} + \frac{\overline{A}/2}{V_p} \right]$$

$$V_o = \frac{-R_L\ g_{mo}}{V_p}\ A\ B \qquad \text{where} \quad g_{mo} = \frac{-2I_{dss}}{V_p} \tag{5.22}$$

$$V_o = \frac{2R_L\ I_{dss}}{V_p^{\,2}}\ A\ B \tag{5.23}$$

This shows that for a transconductance multiplier in which the differential pairs are well matched, the output is indeed the product of the inputs and is scaled by the conversion gain factor $2\ R_L\ I_{dss}/V_p^{\,2} = -g_{mo}\ R_L/V_p$.

For proper operation, the saturation current in the top four transistors should be half the saturation current in Transistors Q5 and Q6. I_{dss} in (5.23) is that of Q1 through Q4.

If we let Q5 and Q6 have I_{dss} = 22 mA and V_p = 1 V, similar to Dexcel device D4, then I_{dss} in (5.23) will be 11 mA with

$A = 0.01$ V

$B = 0.5$ V

$R_L = 250$ ohms

$V_o = 2\ (11 \times 10^{-3})\ (250)\ (0.01)\ (0.5) = 0.0275$ V

When A and B are the amplitudes of a sinewave, their product yields the sum and difference frequencies with a magnitude AB/2 or 0.0138 V. This value was compared with a value computed using SPICE. Since SPICE uses a square law model for JFETs, the data from the DXL2503s easily fit the model in SPICE.

Tables 5-5 and 5-6 specify the model parameter values for devices D2 and D4. The dc characteristics are defined by the parameters VTO and beta, which determine the variation of drain current with gate voltage. The graphs in Appendix D are a plot of V_{gs} vs $\sqrt{I_d}$. The slope of this line is $\sqrt{beta}$ and the V_{gs} axis intercept is VTO. CGS and CGD are the gate-to-source capacitance and the gate-to-drain capacitance respectively. RS is the source ohmic resistance and RD is the drain ohmic resistance.

For Device D4

VTO = 1

Beta = 22×10^{-3}

CGS = 0.02 pF

CGD = 0.06 pF

RD = 3.4 ohms

RS = 2 ohms

These values of capacitance and resistance were chosen to give a comparison between the performance of the various multiplier configurations. They do not necessarily give the proper gain slope with frequency.

Table 5-5. SPICE JFET Model Parameters for Device D2

V_g	I_d	$\sqrt{I_d}$	V_{TO}
0	41.2	6.42	2.1 V
0.5	24.7	4.97	
-1	10.8	3.29	
-1.5	3.38	1.84	

Average value of $\sqrt{B}$ = 3.05

Table 5-6. SPICE JFET Model Parameters for Device D4

V_g	I_d	$\sqrt{I_d}$	V_{TO}
0	22.46	4.74	1.0 V
0.25	12.68	3.56	
0.3	10.55	3.25	
0.5	5.21	2.28	
0.75	1.2	1.10	
1	0.14	0.37	

$\sqrt{B} = 5$

The variable transconductance multiplier was simulated using a 10 mV, 10 GHz RF and a 0.5 V, 6 GHz LO. SPICE performed a fourier analysis using 2 GHz as the fundamental frequency. The first nine components were calculated. The amplitude of the difference frequency at 4 GHz is 12.28 mV. The amplitude of the sum frequency at 16 GHz is 9.4 mV. Clearly, we see that the gain is rolling off with frequency. The analysis predicts a 13.8 mV amplitude at midband frequencies. The simulation using SPICE and the analysis correlate well. SPICE shows excellent suppression of the LO and RF components. The dc bias conditions are given. A typical biasing configuration uses +9 V as the drain supply, +3 V as a gate supply, and -0.5 V as a gate supply. The total power dissipation is 95 mW. A printout of the SPICE analysis is shown in Appendix D.

5.3.2 Analysis of Analog Multiplier Design No. 2

The top four transistors in Figure 5-12 are biased in their saturation region, while the bottom four transistors are biased in their linear region. Thus in order to analyze the multiplier, one must first obtain I vs V characteristics for the transistors operating in their respective regions. The analysis is as follows.

I_1 in Figure 5-12 can be determined using

$$I_1 = g_{ds1} V_{ds1} \tag{5.24}$$

We will next show that

$$V_{ds1} = B\left(\frac{g_{m5}}{g_{m5} + g_{ds1}}\right) \tag{5.25}$$

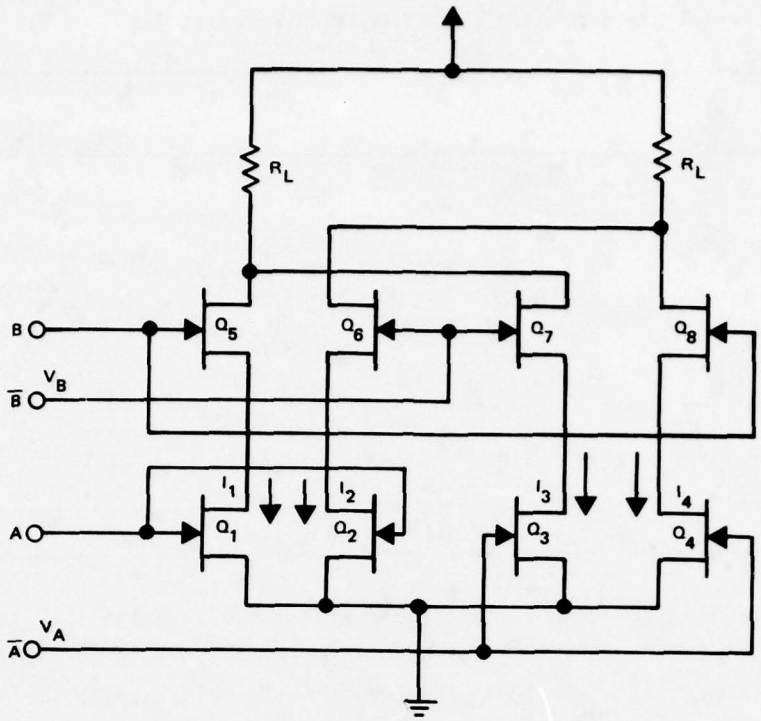


Figure 5-12. Analog Multiplier Design No. 2

where g_{ds1} is the drain to source resistance of Q1 while in its linear region and g_{m5} is the transconductance of Q5.

A simple model for an unsaturated FET is a voltage variable conductance (resistance) as shown in Figure 5-13. Two simple gate FETs in cascode, Q1 and Q2, are shown in Figure 5-14a. In Figure 5-14b, a simple model is given for Q1 saturated, and Q2, unsaturated. Writing node equations to solve for V_1 in Figure 5-14b.

$$V_1 \, g_{ds1} - g_m \, V_{gs2} = 0 \tag{5.26}$$

$$\frac{V_2}{R_d} + g_m \, V_{gs2} = 0 \tag{5.27}$$

substituting $V_{gs2} = B - V_1$

$$V_1 \left[g_{ds1} + g_m \right] = g_m \, B \tag{5.28}$$

$$V_1 \left[-g_m \right] + V_2 \left[\frac{1}{R_D} \right] = -g_m \, B \tag{5.29}$$

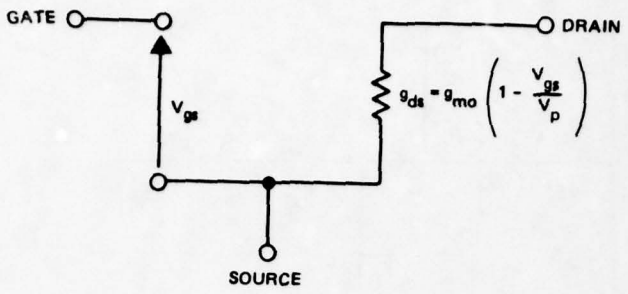


Figure 5-13. Unsaturated FET Model

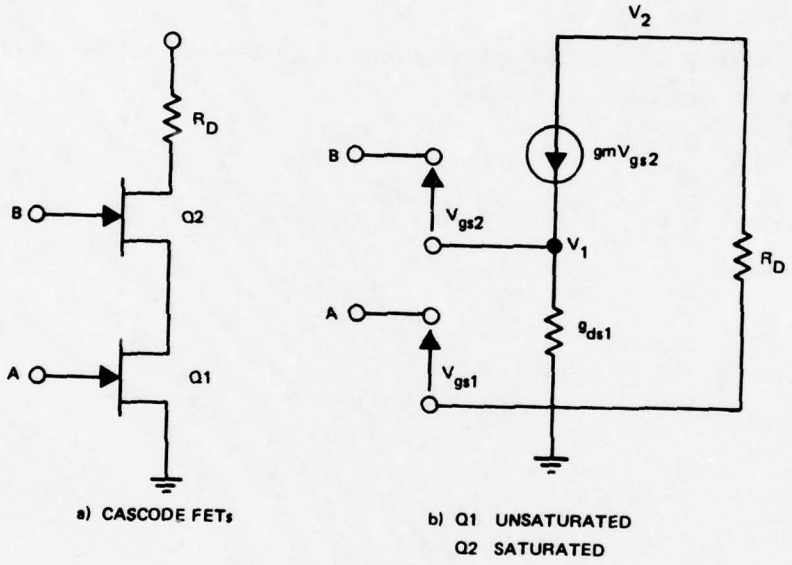


Figure 5-14. Cascode FETS and Equivalent Model

in matrix form

$$\begin{bmatrix} g_{ds1} + gm & 0 \\ -g_m & \frac{1}{R_D} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} g_m B \\ -g_m B \end{bmatrix}$$

solving for V_1

$$V_1 = \frac{\begin{vmatrix} g_m & 0 \\ -g_m B & \frac{1}{R_D} \end{vmatrix}}{\begin{vmatrix} g_{ds1} + g_m & 0 \\ -g_M & \frac{1}{R_D} \end{vmatrix}} = \frac{\frac{1}{R_D}\left[g_m B\right]}{\frac{1}{R_D}\left[g_{ds1} + g_m\right]}$$

$$V_1 = \left[\frac{g_m}{g_m + g_{ds1}}\right] B \tag{5.30}$$

V_1 is the drain voltage of the voltage variable conductance. This establishes the desired relation of equation (5.25) that

$$V_{ds1} = B\left(\frac{g_{m5}}{g_{m5} + g_{ds1}}\right) \tag{5.25}$$

Now, for

$$g_m >> g_{ds1} \tag{5.31}$$

$$\frac{g_m}{g_m + g_{ds1}} \simeq 1$$

therefore

$$V_{ds1} = B \tag{5.32}$$

Equation (5.31) places a restriction on g_m and g_{ds1}. If this restriction is met, g_{ds1} linearizes Q5's response — an asset. Substituting (5.32) into (5.24)

$$I_1 = g_{do}\left(1 - \frac{A}{V_p}\right) B \tag{5.33}$$

and

$$I_2 = g_{do}\left(1 - \frac{A}{V_p}\right) \overline{B} \tag{5.34}$$

$$I_3 = g_{do}\left(1 - \frac{\overline{A}}{V_p}\right)\overline{B} \tag{5.35}$$

$$I_4 = g_{do}\left(1 - \frac{\overline{A}}{V_p}\right)B \tag{5.36}$$

$$V_o = \left[\left(I_1 - I_2\right) + \left(I_3 - I_4\right)\right] R_L \tag{5.37}$$

$$V_o = \left[\left(2\, g_{do}\, B - 2\, g_{do}\, \frac{AB}{V_p}\right) + \left(-2\, g_{do}\, B - 2\, g_{do}\, \frac{AB}{V_p}\right)\right] R_L$$

$$V_o = \frac{-4\, g_{do}\, R_L}{V_p}\, AB \tag{5.38}$$

where

$$g_{do} = \frac{-2\, I_{dss}}{V_p}$$

$$V_o = \frac{8\, I_{dss}\, R_L}{V_p^{\,2}}\, A\, B \tag{5.39}$$

If this multiplier were driven by signal generators B/2, $\overline{B}/2$ and A/2, $\overline{A}/2$ as was done in the variable transconductance multiplier, (5.39) would have to be divided by 4, yielding

$$V_o = \frac{2\, I_{dss}\, R_L}{V_p^{\,2}}\, A\, B \tag{5.40}$$

At first it would appear that this multiplier has the same gain as the variable transconductance multiplier. There is one problem, however. The I_{dss} in (5.40) is the saturation current of the voltage variable resistors Q1 through Q4. According to (5.31)

$$g_{m\ 5,\ 6,\ 7,\ 8} >> g_{ds\ 1,\ 2,\ 3,\ 4}$$

which implies that

$$I_{dss\ 5,\ 6,\ 7,\ 8} >> I_{dss\ 1,\ 2,\ 3,\ 4}$$

But this can't be, because the same current that flows in the upper transistors must flow in the lower ones. Consequently, we decided that it was not practical to build this multiplier.

Analog multiplier design No. 3 (resistive modulated multiplier) is feasible because the voltage variable resistors do not have to sink the same current that the saturated transistors do. Design No. 3 uses active current sources to overcome the inherent problems in design No. 2.

5.3.3 Resistive Modulated Multiplier

The currents in Figure 5-15 are given by

$$I_1 = I_o + I_5 \tag{5.41}$$

$$I_2 = I_o - I_5 \tag{5.42}$$

$$I_1 - I_2 = 2I_5 \tag{5.43}$$

$$I_3 = I_o + I_6 \tag{5.44}$$

$$I_4 = I_o - I_6 \tag{5.45}$$

$$I_3 - I_4 = 2I_6 \tag{5.46}$$

$$V_o = \left[\left(I_1 - I_2 \right) + \left(I_3 - I_4 \right) \right] R_D \tag{5.47}$$

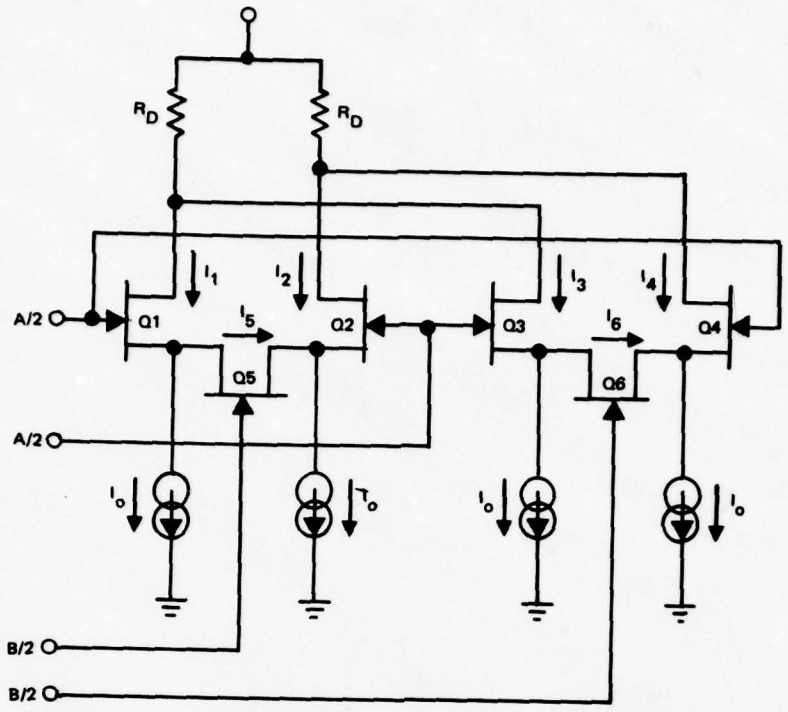


Figure 5-15. Resistive Multiplier Schematic

substituting (5.43) and (4.46) into (5.47)

$$V_o = \left[I_5 + I_6 \right] 2R_D \tag{5.48}$$

$$I_5 = g_{ds5} V_{ds5} \tag{5.49}$$

where g_{ds5} is source to drain conductance of Q5 and V_{ds5} is source to drain voltage of Q5.

$$g_{ds5} = g_{do} \left(1 - \frac{V_{gs5}}{V_p} \right) = g_{do} \left(1 - \frac{B/2}{V_p} \right) \tag{5.50}$$

$$V_{ds5} = 1/3 \left(\frac{A}{2} - \frac{\overline{A}}{2} \right) = 1/3\ A \qquad \text{(see Appendix D for derivation)} \tag{5.51}$$

$$I_5 = \frac{1}{3} g_{do} \left(1 - \frac{B/2}{V_p} \right) A \tag{5.52}$$

$$I_6 = g_{ds6}\, V_{ds6} \tag{5.53}$$

$$g_{ds6} = g_{do}\left(1 - \frac{\overline{B}/2}{V_p}\right) \tag{5.54}$$

$$V_{ds6} = 1/3\left(\frac{\overline{A}}{2} - \frac{A}{2}\right) = -\,1/3\ A \tag{5.55}$$

$$I_6 = -\frac{1}{3}\, g_{do}\left(1 - \frac{\overline{B}/2}{V_p}\right) A \tag{5.56}$$

substituting (5.52) and (5.56) into (5.48)

$$V_o = \left[I_5 + I_6\right] 2R_D \tag{5.57}$$

$$= \left[g_{do}\left(1 - \frac{B/2}{V_p}\right) - g_{do}\left(1 - \frac{\overline{B}/2}{V_p}\right)\right] \frac{1}{3}\, R_D\, A$$

$$V_o = \left[-g_{do}\ \frac{B}{V_p}\right] \frac{2}{3}\, R_D\, A \tag{5.58}$$

$$V_o = \frac{-2\, g_{do}\, R_D}{3\, V_p}\ AB$$

where

$$g_{do} = \frac{-2I_{dss}}{V_p}$$

$$V_o = \frac{4I_{dss}\, R_D}{3\, V_p^{\,2}}\ AB \tag{5.59}$$

The midband analysis of the resistive multiplier predicts that

$$V_o = \frac{4\ I_{dss}\, R_D}{3\, V_p^{\,2}}\ A\ B$$

It should have 3.5 dB less output voltage than the variable transconductance multiplier.

If the LO is much smaller than V_p, the drain conductance of the voltage variable resistors should be approximately equal to the transconductance of the saturated transistors.

If we let

$$LO = 0.1 \text{ V}$$

$$RF = 0.01 \text{ V}$$

$$V_p = 1 \text{ V}$$

$$I_{dss} = 10 \text{ mA}$$

$$R_p = 250 \text{ ohms}$$

then

$$V_o = \left(\frac{4}{3}\right)(11)\ (0.25)\ (0.01)\ (0.1) = 3.667 \text{ mV}$$

If A and B are sinewaves

$$V_o = \frac{3.662}{2} = 1.83 \text{ mV}.$$

5.3.4 Conclusions

The analysis shows that both the variable transconductance multiplier and the resistive modulated multiplier should function well as analog multipliers. Best performance of the transconductance multiplier will be realized when the drain current in the saturation region has a square law dependence on gate voltage. This has been theoretically and experimentally been shown to be the case for FETs fabricated on uniform epi for gate lengths as short as one half micron. Best performance of the variable resistance multiplier is expected when the FET conductance in the linear region has a first order dependence on gate voltage. This has also been found (experimentally) to be the case for uniform epi devices.

6. PROCESS AND DEVICE DESIGN EVALUATION

To evaluate the design and processing techniques developed during the first phase of this work, three types of active chips were fabricated and tested. The following figures and tables report the test results for the discrete FET devices, the discrete TED devices, and the analog multiplier chips.

6.1 DISCRETE FET DEVICES

The discrete FETs are fabricated with an ion-implanted channel and have a gate 1 micron by 250 microns. The drain current vs drain voltage curves are shown for nine devices in Figures 6-1 through 6-9. In the figures, the solid lines are the data as measured for various gate voltages. The curves were traced manually using an X-Y recorder.

The drop down in current near I_{dss} for large drain voltages does not indicate a negative resistance region, but rather appears to be due to a heating effect that occurs as the voltage is increased from 0 V to 6 V. Comparison of the following noise figure data with the dc data will show that the steady-state value of I_{dss} is lower than the values indicated by the swept voltage measurements.

The individual points superimposed on the dc curves in Figures 6-1 through 6-9 are obtained from the computer modeling. In each case, the doping concentration was varied slightly to match I_{dss} for each device, all other parameters are constant.

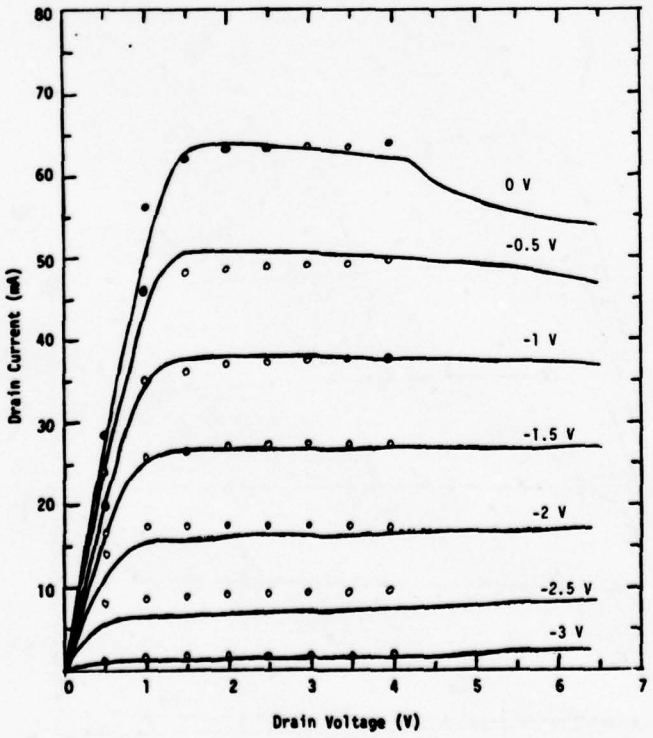


Figure 6-1. Device 7-1 DC Characteristics

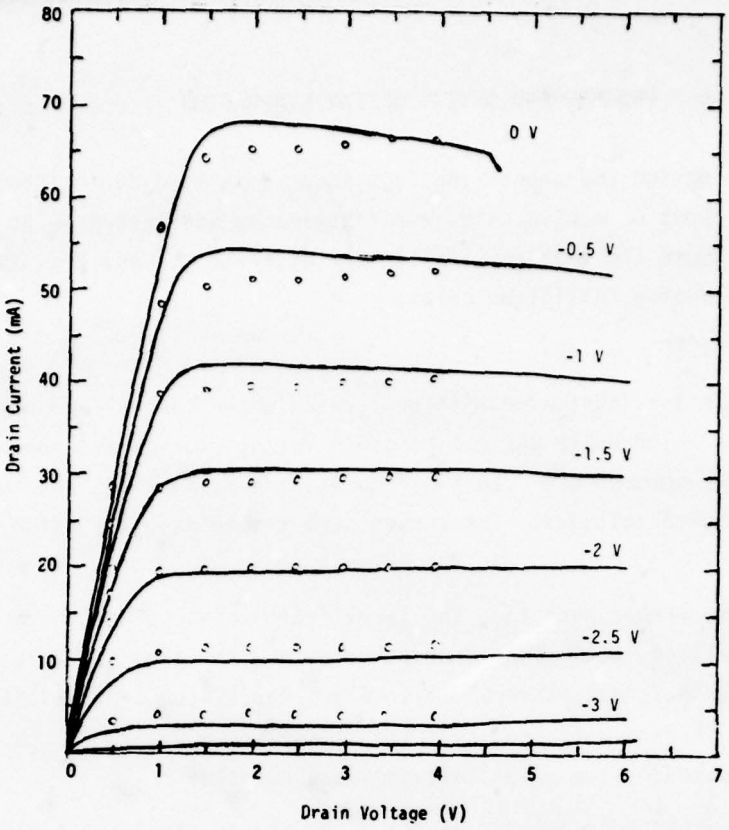


Figure 6-2. Device 7-2 DC Characteristics

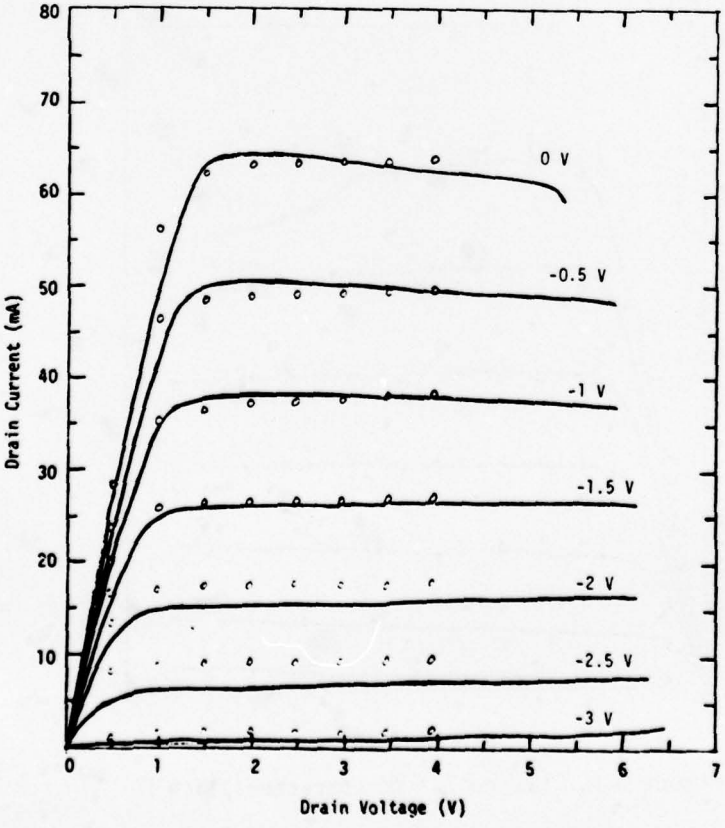


Figure 6-3. Device 7-3 DC Characteristics

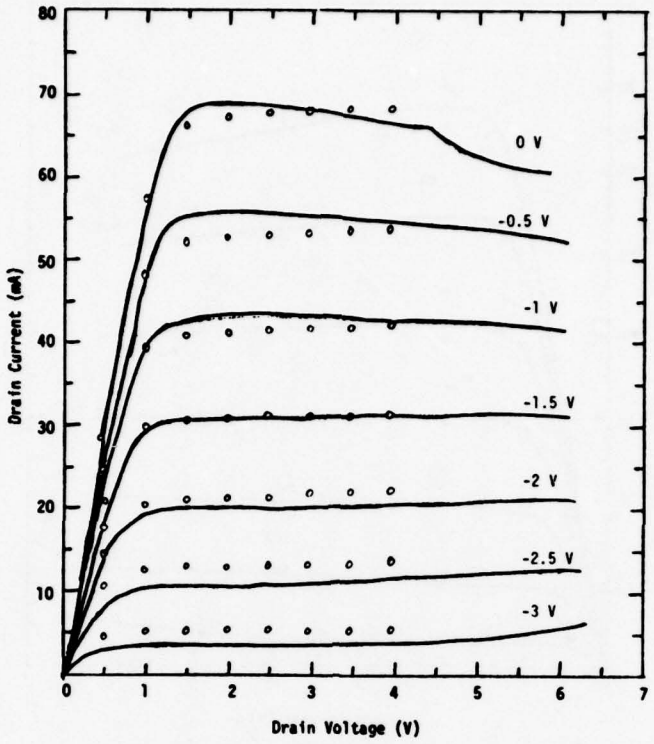


Figure 6-4. Device 7-4 DC Characteristics

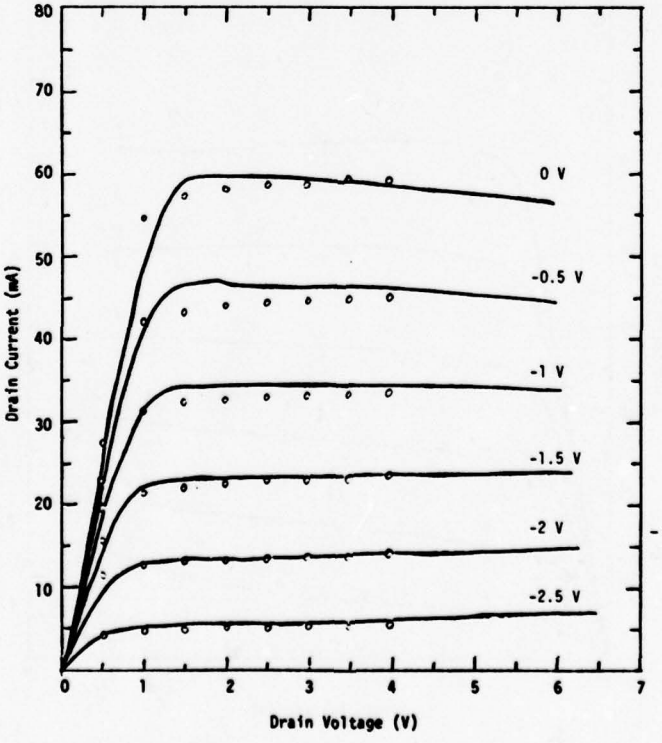


Figure 6-5. Device 7-5 DC Characteristics

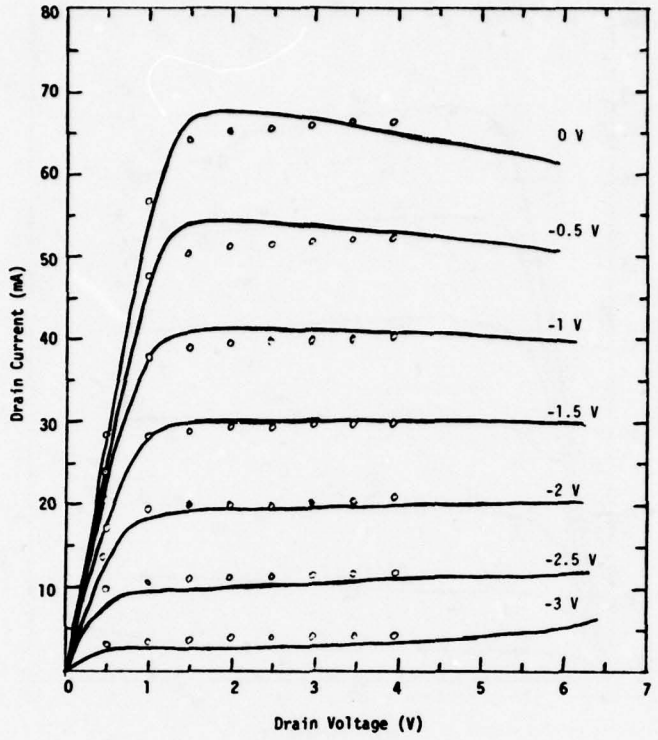


Figure 6-6. Device 7-6 DC Characteristics

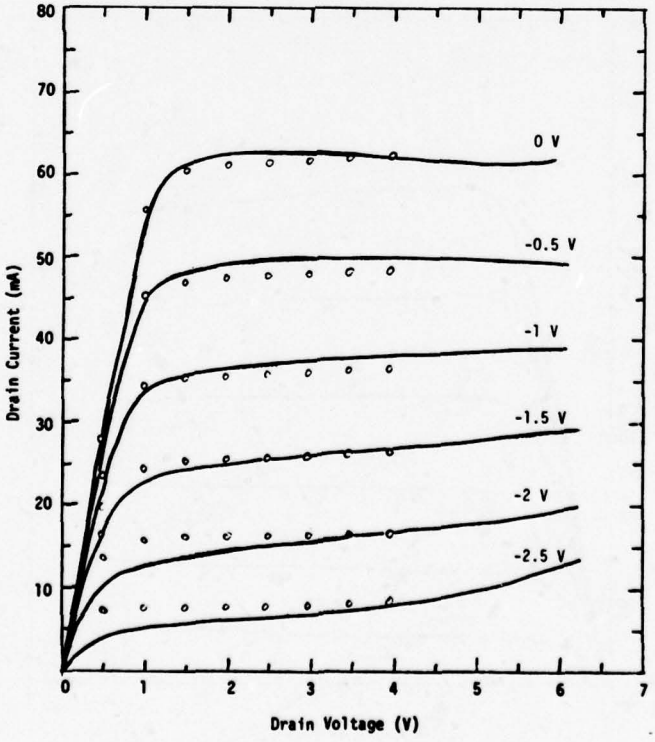


Figure 6-7. Device 8-1 DC Characteristics

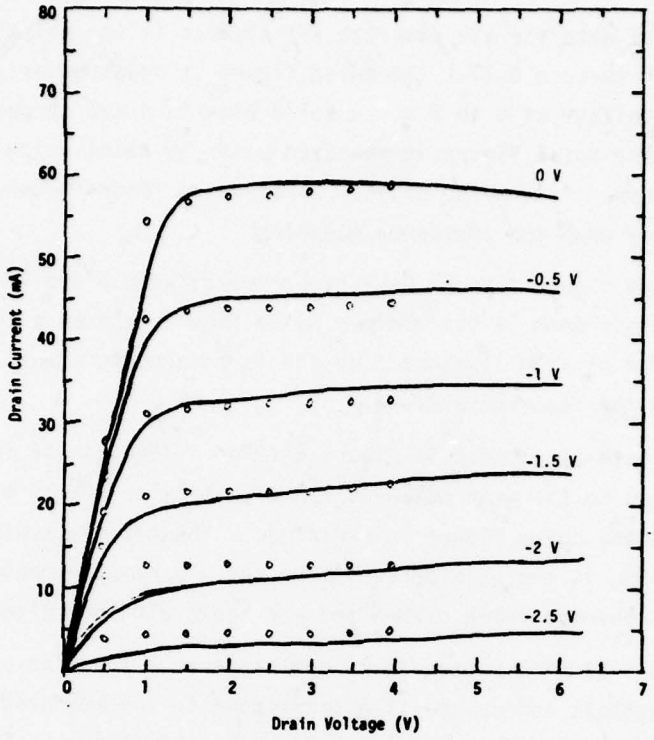


Figure 6-8. Device 8-4 DC Characteristics

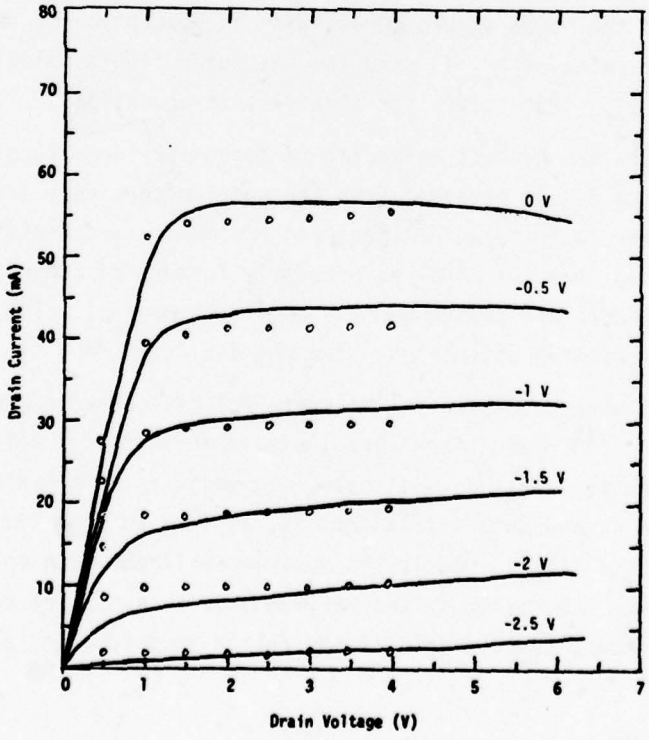


Figure 6-9. Device 8-5 DC Characteristics

The second set of data for the discrete FET devices is the noise figure measurements shown in Figures 6-10 through 6-17. The noise figure is measured as a function of drain current for a drain voltage of 5 to 6 V. A solid line is drawn through the data points at each frequency. The noise figure is measured point by point using an Ailtech system noise moinitor and appropriate noise diode. Slide screw tuners between the device fixture and bias tees are used for impedance matching.

The minimum noise figure for the devices occurs between 5 and 10 mA of drain current. Figure 6-18 plots some of the minimum noise figure data as a function of frequency. At 10 GHz the minimum is about 3 dB and is reduced to about 1 dB at 3 GHz. All measurements are for room temperature.

The associated gain is plotted in Figure 6-19 as a function of frequency. Each data point corresponds to the gain measured for a particular set of matching and bias conditions for which the noise figure is a minimum. The maximum available gain, also plotted on Figure 6-19, is the gain derived from the S-parameter measurements. The points represent the average value of MAG and are shown with one sigma error bars.

Figures 6-20 to 6-24 show noise figure replotted as a function of drain current at 3 and 10 GHz. The symbols and dashed line correspond to the measured data. The solid line is obtained from the computer model. All model parameters are fixed except for the doping concentration which was determined for each sample from the value of I_{dss} obtained from the dc curves. To model the noise figure, the same parameters are used for the dc curves and the noise figure curves with the exception of the source-to-gate resistance. A larger value of R_{sg} is used for the noise figure calculation to account for the reduction in I_{dss} that occurs for steady-state operation.

The model predicts the correct noise figure dependence down to about 10 mA. However, the minimum noise figure obtained from the model occurs very near 0 mA and consequently also is lower than the actual measured minimum. The conclusion to be drawn from this comparison is that the model as presently formulated accurately predicts the noise figure dependence of the device down to about 20% of I_{dss}. The predicted value at 20% of I_{dss} is the minimum noise figure for the device.

The small signal parameters for the discrete FET devices were measured at 25, 50, 75, and 100% of I_{dss}. The measurements are included in Table 6-1 through 6-8. The S-parameters are given in magnitude and angle. In addition, the maximum available gain MAG, stability factor K, and cutoff frequency f_T, as derived from the S-parameters, are also listed. In the tables, MAG is the maximum available gain only if $K \geq 1$. When $K < 1$, the value in the MAG column is the maximum stable gain. The cutoff frequency is the frequency at which the current gain of the device goes to unity as determined from the Y-parameters.

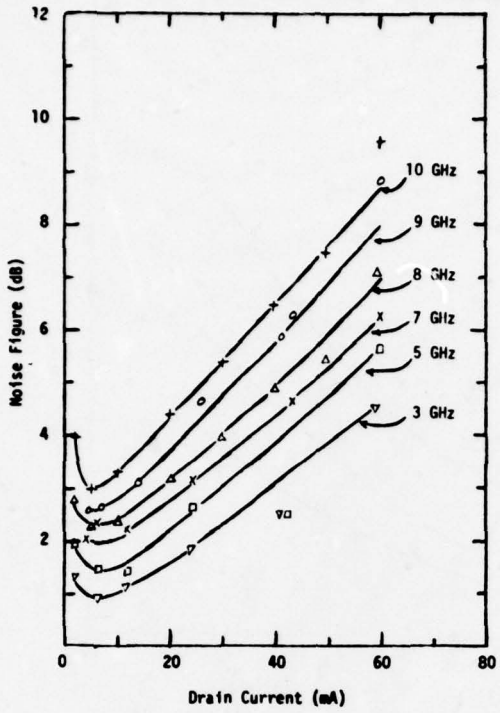


Figure 6-10. Device 7-2 Noise Figure Measurements

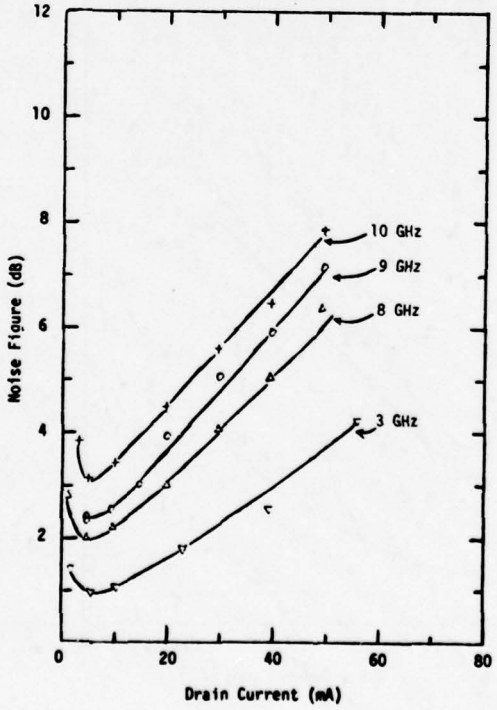


Figure 6-11. Device 7-3 Noise Figure Measurements

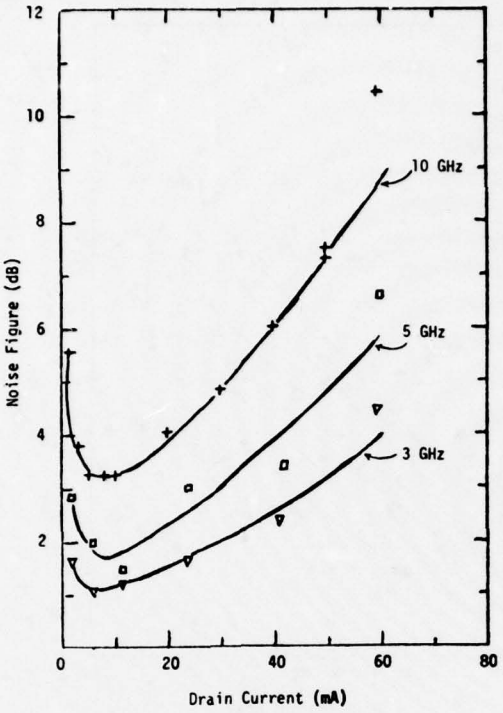


Figure 6-12. Device 7-4 Noise Figure Measurements

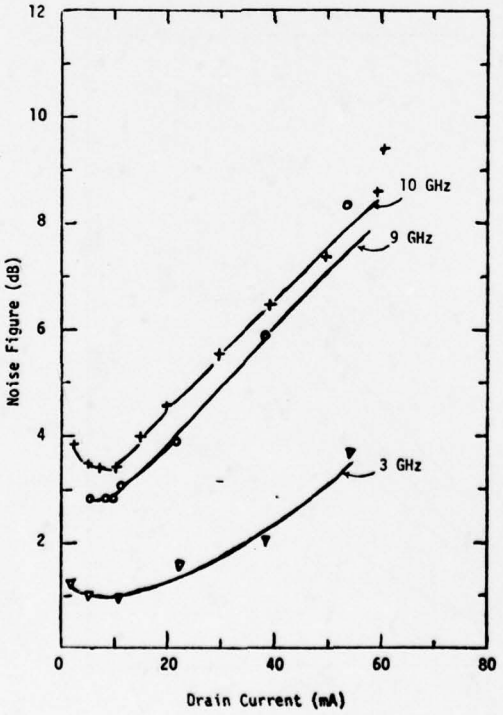


Figure 6-13. Device 7-5 Noise Figure Measurements

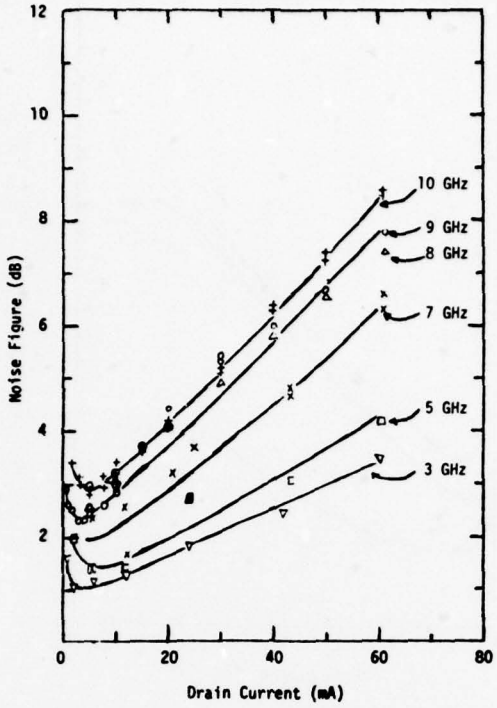


Figure 6-14. Device 7-6 Noise Figure Measurements

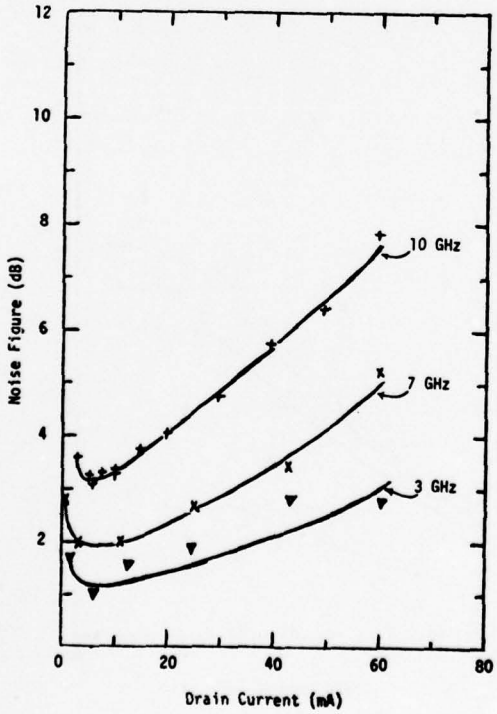


Figure 6-15. Device 8-1 Noise Figure Measurements

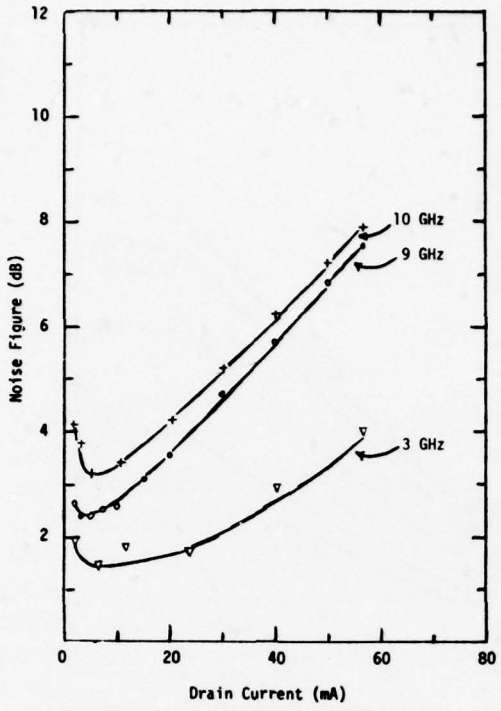


Figure 6-16. Device 8-4 Noise Figure Measurements

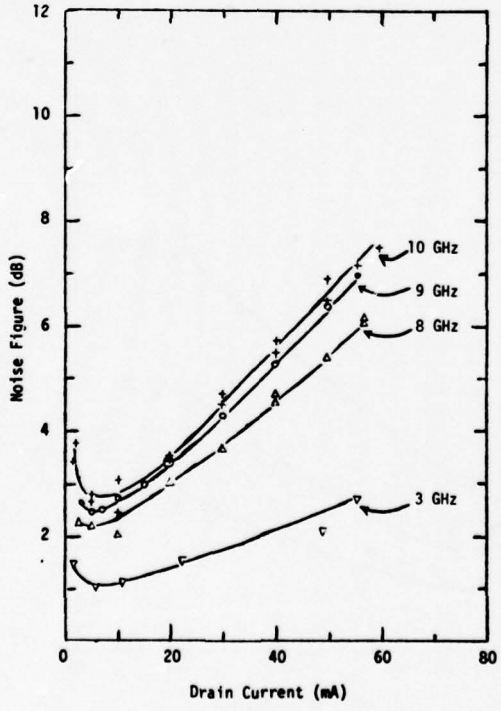


Figure 6-17. Device 8-5 Noise Figure Measurements

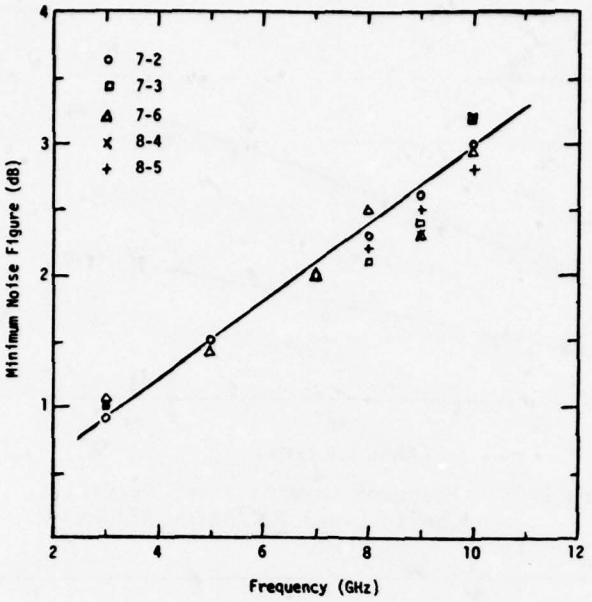


Figure 6-18. Minimum Measured Noise Figure vs Frequency for Discrete 1 Micron FET Devices

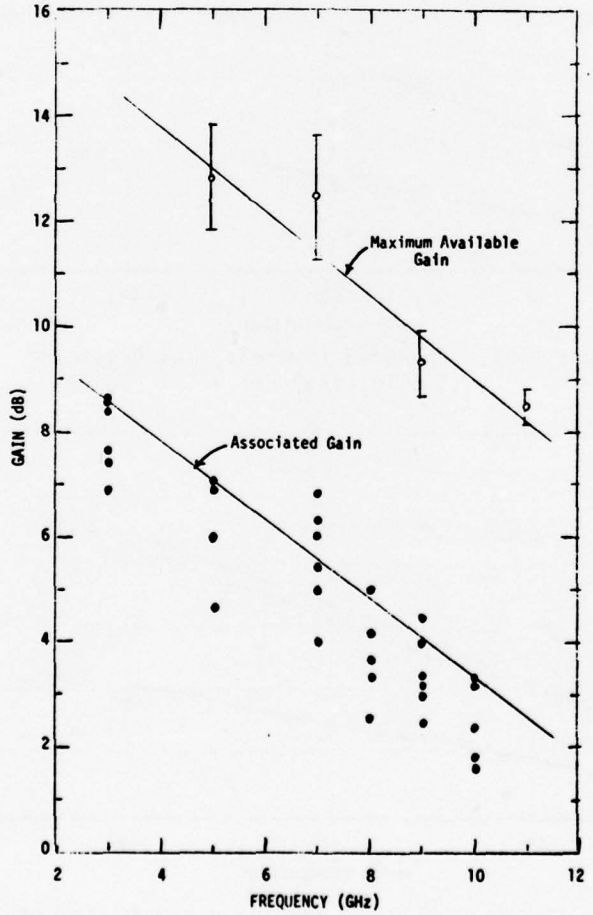


Figure 6-19. Associated Gain and Maximum Available Gain for the Discrete 1 Micron FET Devices

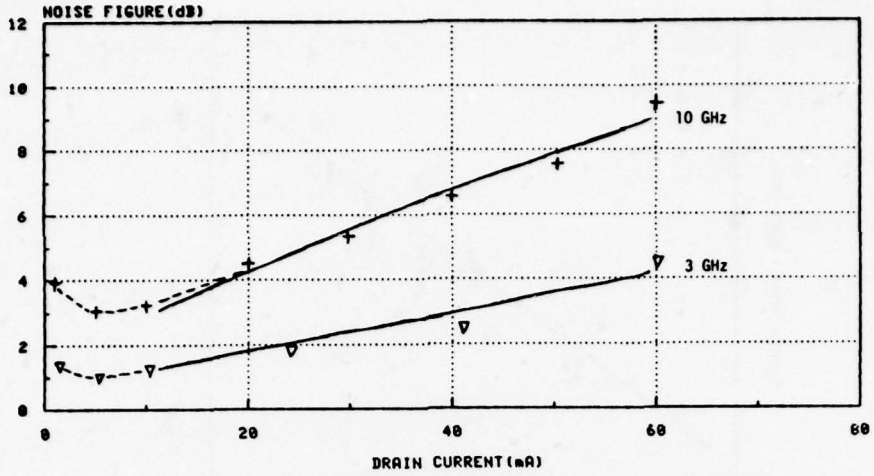


Figure 6-20. Measured (Symbols) and Predicted (Solid Line) FET Noise Figure

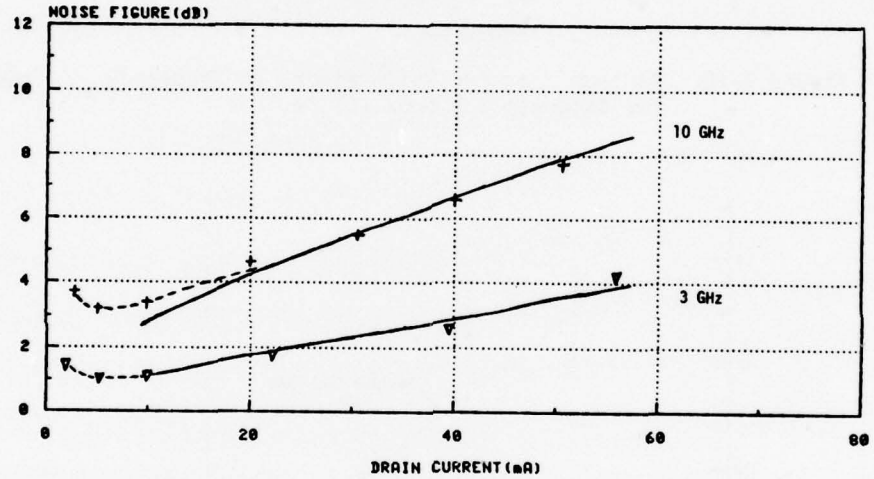


Figure 6-21. Measured (Symbols) and Predicted (Solid Line) FET Noise Figure

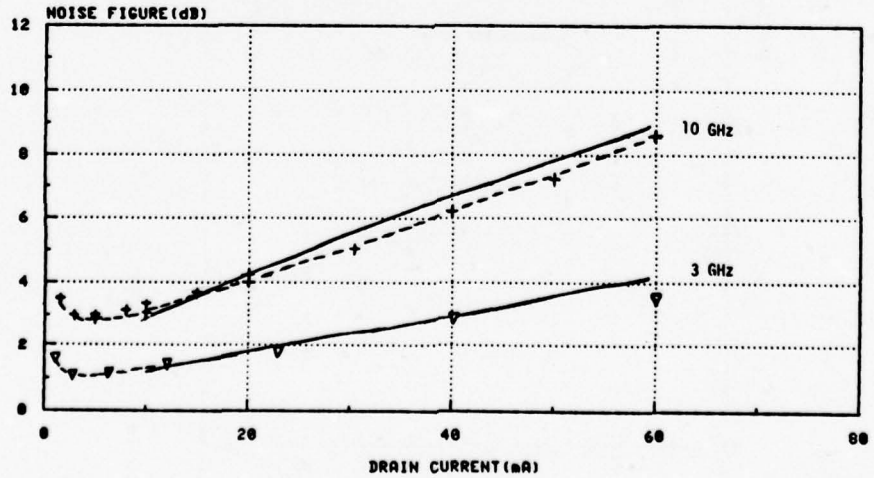


Figure 6-22. Measured (Symbols) and Predicted (Solid Line) FET Noise Figure

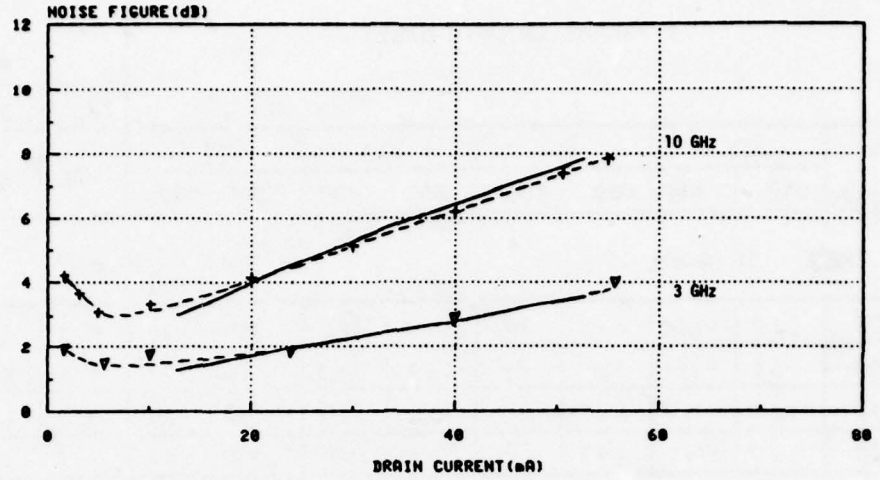


Figure 6-23. Measured (Symbols) and Predicted (Solid Line) FET Noise Figure

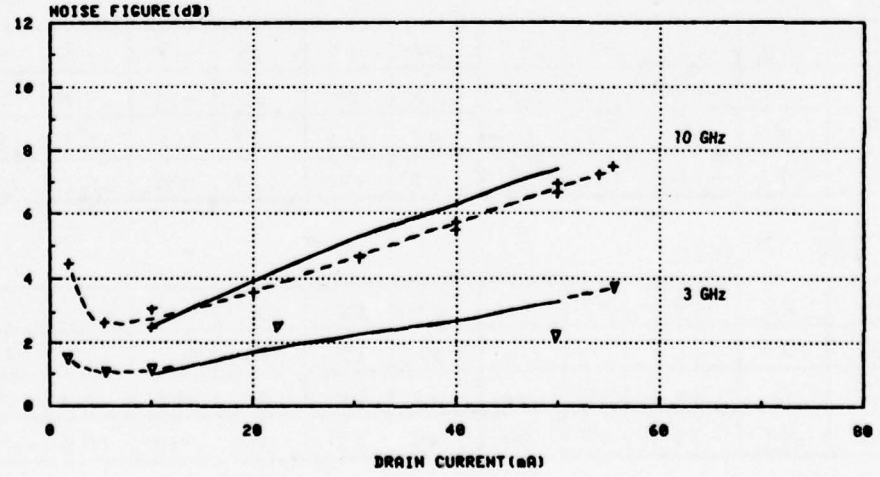


Figure 6-24. Measured (Symbols) and Predicted (Solid Line) FET Noise Figure

Table 6-1. Device 7-2 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 7-2		
									V_{dd} 5 V		
%	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
I_{dss}	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 11 GHz											
25	.63	-135	1.12	82	.03	88	.79	-39	8.2	2.9	9.8
50	.63	-146	1.19	78	.03	127	.81	-37	9.2	2.5	9.9
75	.67	-155	1.19	73	.04	153	.86	-35	12.0	1.2	9.1
100	.67	-164	.93	65	.05	135	.89	-34	12.7	.8	6.9
FREQ. 9 GHz											
25	.67	-96	1.58	84	.04	69	.75	-23	10.4	1.9	13.4
50	.67	-106	1.68	80	.03	104	.78	-21	12.2	1.8	13.1
75	.67	-116	1.78	76	.03	134	.81	-18	14.6	1.3	12.8
100	.67	-127	1.33	70	.04	116	.84	-17	13.7	1.1	8.9
FREQ. 7 GHz											
25	.78	-65	1.55	108	.04	67	.84	-14	13.6	1.1	12.5
50	.75	-74	1.68	104	.03	84	.84	-12	14.4	1.3	12.7
75	.72	-81	1.78	99	.03	128	.89	-10	17.7	.49	11.9
100	.71	-91	1.50	92	.03	120	.89	-10	12.5	1.6	9.1
FREQ. 5 GHz											
25	.84	-58	1.58	112	.04	55	.81	-12	13.2	1.2	9.9
50	.83	-66	1.78	110	.03	58	.84	-11	15.2	1.2	9.8
75	.81	-74	1.78	106	.03	65	.87	-10	17.7	.99	8.9
100	.79	-80	1.55	102	.03	73	.87	-10	15.6	1.1	7.3
FREQ. 3 GHz											
25	.94	-30	1.74	155	.03	81	.84	-6	17.7	.33	12.0
50	.93	-35	2.06	153	.03	82	.87	-5	18.2	.23	11.6
75	.91	-40	2.11	150	.03	83	.89	-4	18.5	.22	10.7
100	.89	-44	2.00	146	.03	98	.89	-4	18.2	.09	9.3

Table 6-2. Device 7-3 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 7-3		
									V_{dd} 5 V		
% I_{dss}	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 11 GHz											
25	.63	-129	1.06	80	.04	89	.79	-53	8.0	2.2	10.0
50	.63	-139	1.12	77	.04	117	.84	-50	10.2	1.5	9.8
75	.67	-147	1.12	72	.04	142	.88	-48	13.5	1.0	9.0
100	.67	-164	.75	63	.06	146	.90	-50	11.0	.9	5.9
FREQ. 9 GHz											
25	.63	-89	1.58	88	.05	60	.72	-19	9.3	2.0	14.6
50	.63	-99	1.68	85	.04	81	.75	-17	10.8	1.9	14.2
75	.63	-106	1.78	82	.03	113	.79	-15	12.6	1.8	14.0
100	.63	-126	1.12	73	.04	136	.84	-16	10.4	1.5	7.7
FREQ. 7 GHz											
25	.79	-64	1.50	109	.04	63	.84	-14	13.2	1.2	12.2
50	.75	-73	1.64	106	.03	71	.84	-12	13.5	1.4	12.1
75	.74	-80	1.78	102	.03	90	.87	-10	17.7	.92	12.1
100	.71	-95	1.27	92	.03	159	.91	-11	16.3	.49	7.4
FREQ. 5 GHz											
25	.84	-58	1.58	113	.05	54	.79	-13	13.2	1.1	10.1
50	.82	-65	1.78	111	..04	56	.81	-12	14.4	1.1	10.2
75	.79	-71	1.78	109	.03	60	.84	-10	14.5	1.3	9.7
100	.79	-86	1.41	100	.03	79	.89	-9	16.7	.90	6.2
FREQ. 3 GHz											
25	.94	-28	1.68	158	.03	83	.84	-3	17.5	.34	12.3
50	.91	-32	1.95	156	.03	83	.84	-2	18.1	.42	12.7
75	.91	-37	2.11	154	.03	83	.85	-2	19.5	.33	11.8
100	.89	-46	1.78	148	.03	88	.89	-2	17.7	.24	7.9

Table 6-3. Device 7-4 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 7-4		
									V_{dd} 5V		
% I_{dss}	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 1 GHz											
25	.65	-124	1.10	93	.04	94	.79	-63	8.7	2.0	11.0
50	.67	-133	1.15	80	.04	124	.81	-62	9.8	1.7	10.8
75	.67	-140	1.15	76	.04	140	.84	-59	10.6	1.5	10.2
100	.69	-153	.84	66	.06	149	.79	-61	6.3	1.8	7.4
FREQ. 9 GHz											
25	.65	-84	1.50	83	.04	66	.72	-29	9.1	2.4	14.6
50	.66	-94	1.58	80	.03	95	.75	-27	10.6	2.4	13.8
75	.66	-102	1.58	77	.03	122	.78	-25	11.7	1.9	12.8
100	.67	-116	1.19	69	.04	135	.78	-25	9.6	1.8	8.8
FREQ. 7 GHz											
25	.79	-60	1.50	109	.04	70	.81	-18	12.7	1.3	13.2
50	.78	-68	1.68	105	.03	84	.84	-16	15.3	1.1	13.1
75	.75	-75	1.78	102	.03	113	.87	-14	17.7	.66	12.7
100	.79	-87	1.41	92	.03	152	.84	-15	16.7	.69	8.9
FREQ. 5 GHz											
25	.84	-56	1.58	114	.04	56	.79	-14	13.0	1.2	10.4
50	.83	-63	1.78	112	.03	59	.81	-13	14.5	1.3	10.4
75	.81	-69	1.78	109	.03	62	.84	-11	15.1	1.2	9.5
100	.79	-83	1.41	103	.03	74	.79	-12	11.9	1.7	6.7
FREQ. 3 GHz											
25	.94	-26	2.51	102	.03	83	.83	-4	19.2	.92	19.5
50	.94	-31	2.82	100	.03	83	.84	-3	19.7	.88	18.3
75	.91	-36	3.09	98	.03	84	.84	-2	21.1	.86	22.4
100	.89	-42	2.66	91	.03	87	.84	-3	19.5	.97	13.0

Table 6-4. Device 7-5 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 7-5		
									V_{dd} 5 V		
% I_{dss}	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 11 GHz											
25	.65	-139	1.06	77	.04	97	.79	-54	8.3	2.1	9.6
50	.63	-151	1.12	72	.04	132	.83	-52	9.4	1.8	9.6
75	.67	-162	1.12	66	.05	148	.87	-49	13.5	.98	8.9
100	.71	-169	.75	58	.06	154	.89	-49	10.9	.95	5.7
FREQ. 9 GHz											
25	.63	-99	1.50	82	.04	65	.72	-21	9.0	2.5	12.8
50	.63	-112	1.58	78	.03	98	.75	-19	10.4	2.5	12.3
75	.63	-123	1.68	74	.05	129	.79	-16	12.3	1.8	12.1
100	.63	-133	1.17	68	.03	139	.81	-16	9.2	2.5	7.9
FREQ. 7 GHz											
25	.76	-69	1.50	107	.04	59	.84	-12	12.4	1.3	11.5
50	.72	-78	1.68	102	.03	71	.84	-10	13.2	1.5	11.8
75	.71	-87	1.78	97	.03	109	.89	-8	17.7	.67	11.3
100	.67	-98	1.35	89	.03	162	.89	-10	16.5	.84	7.9
FREQ. 5 GHz											
25	.84	-60	1.58	112	.04	56	.81	-13	13.5	1.2	9.6
50	.81	-68	1.78	109	.03	59	.84	-12	14.8	1.2	9.7
75	.79	-77	1.78	106	.03	64	.86	-11	16.0	1.1	8.7
100	.78	-86	1.50	100	.03	74	.89	-11	17.0	.91	6.6
FREQ. 3 GHz											
25	.94	-30	2.37	101	.03	81	.84	-3	19.0	.84	12.2
50	.92	-36	2.82	98	.03	81	.84	-2	19.7	.93	15.9
75	.91	-42	3.16	95	.03	92	.87	-2	20.2	.87	15.2
100	.89	-47	2.82	90	.03	85	.87	-2	19.7	.90	12.2

Table 6-5. Device 7-6 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 7-6		
									V_{dd} 5V		
%	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
I_{dss}	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 11 GHz											
25	.60	-147	1.17	74	.06	74	.77	-58	9.0	1.4	11.1
50	.63	-159	1.20	69	.05	95	.79	-56	9.8	1.4	10.6
75	.63	-168	1.19	63	.06	116	.84	-54	13.0	.9	10.1
100	.63	-177	1.00	58	.06	122	.89	-52	8.1	.7	12.2
FREQ. 9 GHz											
25	.63	-101	1.50	105	.14	43	.71	-23	10.3	.80	13.4
50	.63	-115	1.58	101	.10	46	.75	-21	12.0	.81	12.4
75	.63	-125	1.58	97	.08	49	.75	-20	13.0	.94	11.7
100	.63	-135	1.38	93	.06	51	.78	-19	10.7	1.2	9.6
FREQ. 7 GHz											
25	.71	-73	1.58	102	.03	156	.84	-13	17.2	.99	11.8
50	.69	-83	1.68	97	.04	177	.88	-11	16.2	.31	11.1
75	.67	-91	1.78	92	.05	-173	.91	-9	15.5	.23	10.9
100	.63	-101	1.58	87	.06	-170	.91	-10	14.2	.52	9.2
FREQ. 5 GHz											
25	.81	-63	1.58	110	.04	61	.81	-16	13.3	1.2	9.4
50	.79	-71	1.78	107	.03	70	.83	-15	15.0	1.2	9.5
75	.78	-80	1.82	103	.03	88	.85	-13	17.8	.86	8.8
100	.75	-87	1.78	100	.03	108	.88	-12	17.7	.55	8.0
FREQ. 3 GHz											
25	.93	-30	2.51	101	.03	84	.84	-6	19.2	.89	16.9
50	.91	-36	2.82	98	.03	84	.84	-5	19.7	.90	16.0
75	.89	-41	3.16	95	.03	87	.85	-3	20.2	.84	14.3
100	.89	-46	3.16	92	.03	84	.85	-3	20.2	.84	14.3

Table 6-6. Device 8-1 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 8-1		
									V_{dd} 5V		
% I_{dss}	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 11 GHz											
25	.63	-130	1.29	77	.10	53	.65	-48	8.7	1.2	13.1
50	.62	-139	1.33	76	.07	61	.67	-45	8.4	1.5	12.8
75	.62	-148	1.38	74	.06	70	.70	-43	9.3	1.5	12.6
100	.60	-156	1.38	71	.06	78	.71	-42	9.3	1.5	12.5
FREQ. 9 GHz											
25	.63	-90	1.62	82	.10	42	.63	-31	8.5	1.4	15.9
50	.63	-100	1.78	80	.07	48	.63	-29	9.5	1.6	16.3
75	.62	-108	1.78	77	.06	56	.63	-26	9.5	1.8	15.5
100	.60	-117	1.78	74	.04	63	.67	-25	9.8	2.4	14.5
FREQ. 7 GHz											
25	.79	-63	1.58	109	.08	57	.75	-21	13.0	.92	14.1
50	.75	-70	1.78	105	.06	60	.75	-19	12.8	1.1	14.6
75	.72	-76	1.82	102	.05	63	.75	-17	12.2	1.3	14.1
100	.71	-84	1.93	99	.04	66	.78	-16	13.3	1.3	13.5
FREQ. 5 GHz											
25	.84	-54	1.58	115	.08	53	.75	-16	13.0	.91	11.2
50	.81	-60	1.78	113	.06	53	.75	-15	13.3	1.1	11.6
75	.79	-66	1.88	110	.06	54	.75	-14	13.7	1.0	11.3
100	.78	-72	2.06	108	.04	54	.75	-13	13.5	1.3	11.1
FREQ. 3 GHz											
25	.94	-25	2.37	102	.04	82	.81	-7	17.7	.87	19.6
50	.94	-29	2.82	101	.04	81	.81	-6	18.5	.84	20.1
75	.93	-33	2.99	99	.04	80	.82	-6	18.7	.85	18.7
100	.91	-37	3.16	97	.03	79	.82	-6	20.2	.92	17.6

Table 6-7. Device 8-4 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 8-4		
									V_{dd}	5V	
% I_{dss}	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 11 GHz											
25	.56	-139	1.19	76	.08	66	.67	-24	6.5	1.8	11.2
50	.55	-150	1.22	72	.07	80	.71	-22	7.4	1.8	11.0
75	.56	-160	1.19	69	.06	107	.76	-20	8.3	1.6	10.1
100	.56	-171	1.16	64	.06	113	.83	-17	10.9	1.1	9.3
FREQ. 9 GHz											
25	.63	-95	1.58	89	.08	53	.71	-14	9.2	1.4	14.0
50	.62	-106	1.58	87	.06	64	.72	-12	9.6	1.6	13.0
75	.62	-114	1.62	84	.04	81	.78	-9	11.1	1.7	12.2
100	.60	-127	1.58	81	.04	102	.81	-7	12.1	1.4	11.2
FREQ. 7 GHz											
25	.71	-65	1.41	108	.06	60	.78	-12	9.8	1.4	12.1
50	.71	-73	1.58	105	.04	64	.79	-10	11.2	1.7	12.2
75	.67	-81	1.58	101	.03	72	.83	-8	11.7	1.9	11.1
100	.63	-89	1.58	97	.03	86	.85	-7	12.3	1.7	10.4
FREQ. 5 GHz											
25	.79	-52	1.50	112	.07	52	.75	-14	10.5	1.2	11.1
50	.78	-58	1.62	110	.06	54	.77	-13	11.5	1.2	10.8
75	.75	-64	1.78	107	.04	56	.79	-11	12.3	1.5	10.7
100	.74	-72	1.78	104	.03	59	.81	-10	12.7	1.7	9.6
FREQ. 3 GHz											
25	.91	-28	1.58	155	.04	79	.79	-7	16.0	.56	12.2
50	.90	-32	1.78	153	.04	79	.79	-6	16.5	.54	12.1
75	.89	-36	2.00	151	.03	79	.82	-5	18.2	.58	11.8
100	.87	-41	2.11	148	.03	79	.84	-4	18.5	.57	10.9

Table 6-8. Device 8-5 S-Parameter Data

S-PARAMETER DATA SHEET									DEVICE 8-5		
									V_{dd} 5V		
%	S_{11}		S_{21}		S_{12}		S_{22}		MAG	K	f_T
I_{dss}	mag	ang	mag	ang	mag	ang	mag	ang			
FREQ. 11 GHz											
25	.63	-142	1.23	74	.06	66	.71	-54	8.4	1.7	11.8
50	.63	-151	1.26	71	.04	84	.72	-52	8.3	2.5	11.5
75	.63	-159	1.23	67	.04	108	.77	-50	9.0	2.1	10.7
100	.63	-169	1.19	62	.04	131	.83	-47	10.0	1.7	9.8
FREQ. 9 GHz											
25	.68	-101	1.60	82	.06	53	.71	-21	9.9	1.5	13.3
50	.67	-110	1.74	80	.06	67	.72	-19	11.5	1.3	13.7
75	.65	-118	1.74	77	.04	87	.76	-17	12.0	1.5	12.9
100	.63	-128	1.68	74	.04	113	.84	-15	16.2	.90	11.5
FREQ. 7GHz											
25	.75	-69	1.68	108	.06	62	.78	-14	12.8	1.1	13.7
50	.71	-77	1.78	105	.04	69	.79	-12	12.7	1.4	13.2
75	.71	-85	1.78	101	.03	84	.81	-10	13.5	1.5	12.0
100	.63	-94	1.78	96	.03	112	.87	-8	16.4	1.0	11.2
FREQ. 5 GHz											
25	.84	-53	1.69	115	.06	54	.75	-12	13.0	1.1	12.0
50	.81	-60	1.78	112	.05	56	.76	-11	13.0	1.2	11.4
75	.79	-66	1.88	110	.03	58	.79	-10	13.6	1.6	10.8
100	.78	-74	2.00	106	.03	62	.82	-8	14.9	1.3	10.3
FREQ. 3 GHz											
25	.94	-27	2.51	102	.06	26	.84	-4	16.2	.93	16.3
50	.93	-32	2.82	106	.04	26	.82	-4	18.5	.98	16.4
75	.92	-36	3.04	98	.03	26	.84	-3	19.1	1.0	16.1
100	.89	-41	3.16	95	.03	26	.84	-2	18.4	1.1	14.8

The S-parameter data is summarized in Figures 6-25, 6-26, and 6-27. The averages over eight samples are plotted for the 25% I_{dss} measurements. The open symbols are the average measured values and corresponding one sigma values. The closed symbols are the values computed using the computer model. Figures 6-25 and 6-26 indicate the good agreement for S_{21} and S_{12}. Figure 6-27 compares measured and computed values of S_{11} and S_{22}.

The discrete devices tested are uniform in dc, small signal, and noise figure characteristics. Comparisons between the FET model predictions and the measured data indicate that improvements made in the model during the past work phase have resulted in a reasonably accurate device model.

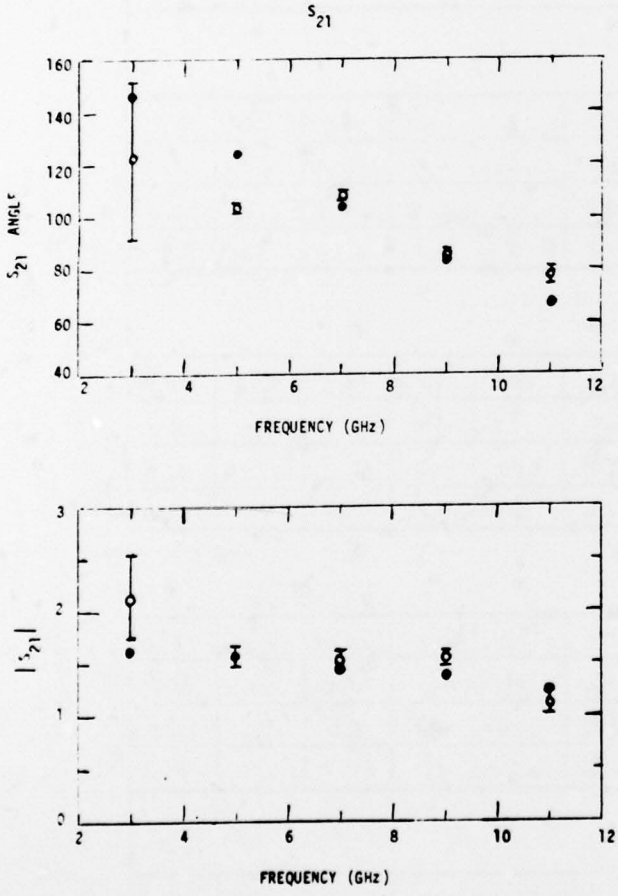


Figure 6-25. Average Measured Values of S_{21} (Open Symbols), One Sigma Standard Deviation, and Predicted Values (Closed Symbols) as a Function of Frequency

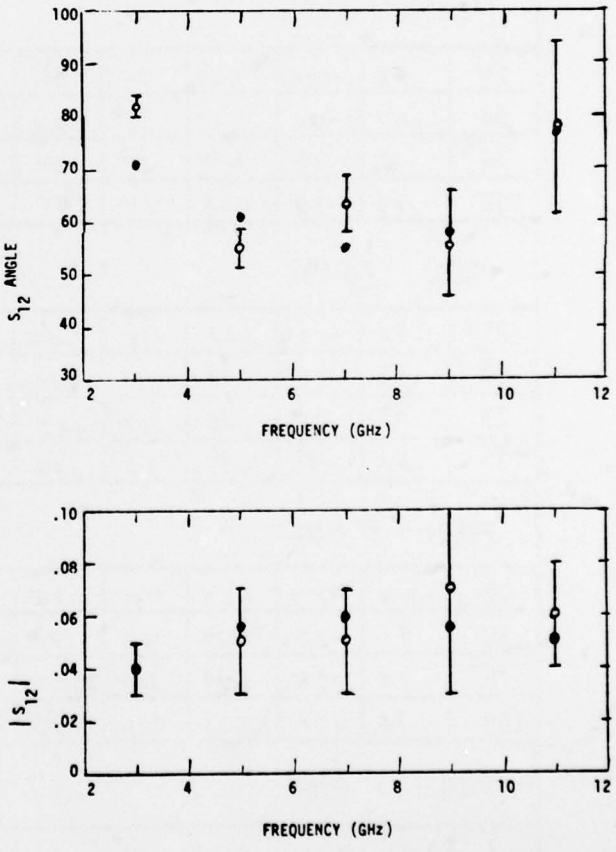


Figure 6-26. Average Measured Values of S_{12} (Open Symbols), One Sigma Standard Deviation, and Predicted Values (Closed Symbols) as a Function of Frequency

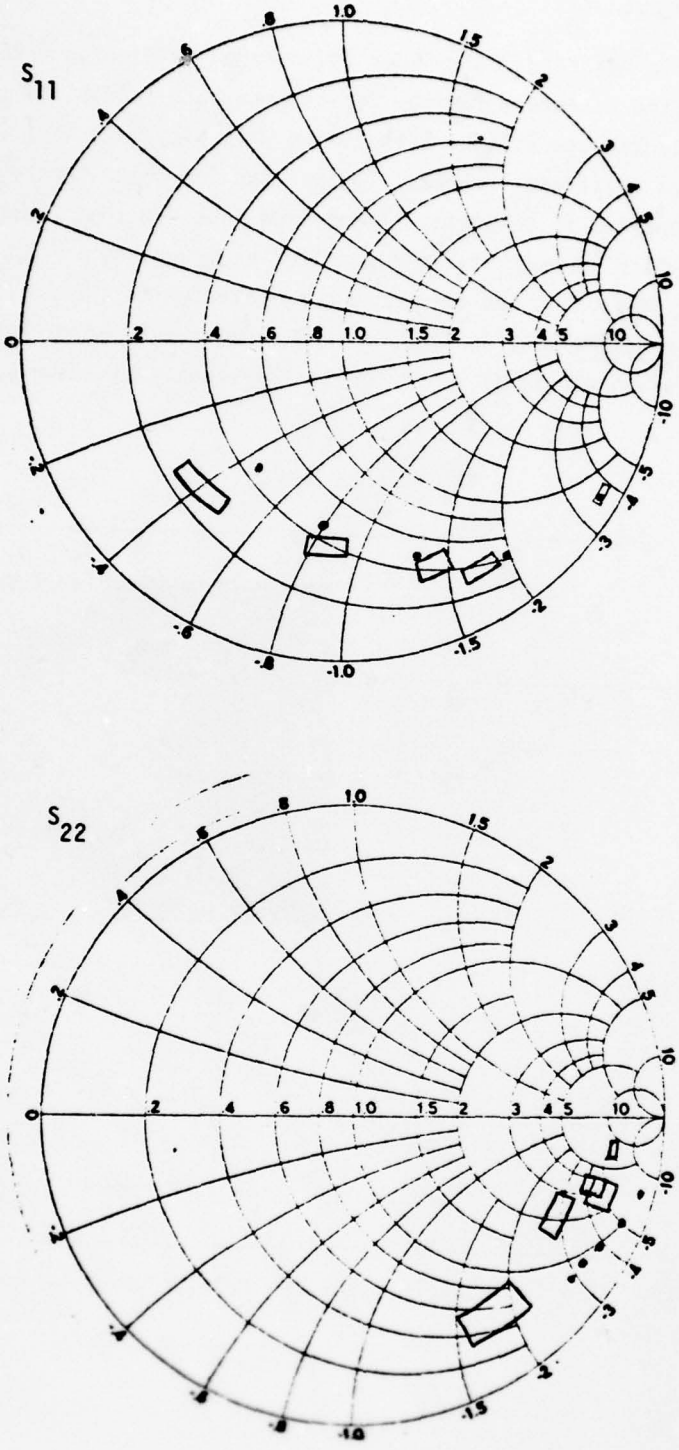


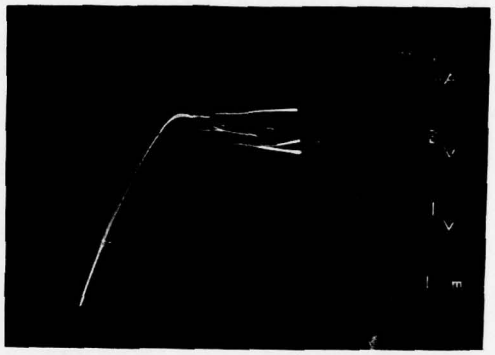
Figure 6-27. Average Measured Values of S_{11} and S_{22} with One Sigma Deviation (Boxes) and Predicted Values (Closed Symbols)

6.2 DISCRETE TED DEVICES

Test data for five discrete TED devices is included in Figures 6-28 through 6-32. Each figure includes the dc curves for the device, the bias conditions for self-oscillation, and injection-locked operation. Each device will oscillate at 5 GHz when properly biased in the negative resistance region. To test the injection-locked operation, a signal at 10 GHz is applied to the gate. The device locks to that integer fraction of the input frequency which is near its self-oscillation frequency. A locking bandwidth is then determined by measuring the frequency range over which the device remains locked to the injected signal. The data in Figures 6-28 through 6-32 gives the locking bandwidth as a function of input signal level for this frequency dividing operation.

$f_{in} = 2 \times f_o$

POWER IN [dBm]	$-\Delta f_o$ [MHz]	$+\Delta f_o$ [MHz]	LOCKING BW [MHz]
-18	20	30	50
-15	24	32	56
-12	30	66	96
-9	32	96	128
-6	32	140	172
-3	32	350	382
0	32	>450	
+3	32	>450	



V_{AC}	10.6 V
V_G	-1.55 V
I_{AC}	6.35 mA
f_o	5.06 GHz

Figure 6-28. TED T5A-1 Self-Oscillating, DC, and Injection-Locked Operation

V_{AC}	11.5 V
V_G	-3.4 V
I_{AC}	6.8 mA
f_o	5.0 GHz

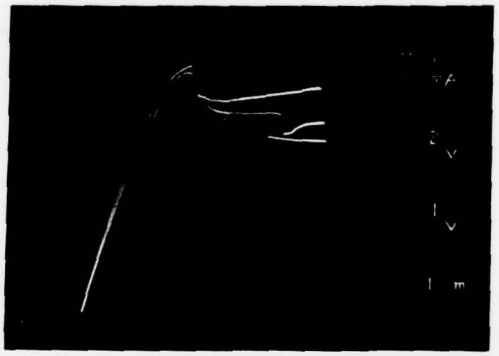
$f_{in} = 2 \times f_o$

POWER IN [dBm]	$-\Delta f_o$ [MHz]	$+\Delta f_o$ [MHz]	LOCKING BW [MHz]
-18	18	43	61
-15	30	50	80
-12	50	70	120
-9	102	105	207
-6	105	140	245
-3	140	200	345
0	110	280	390
+3	220	420	640

Figure 6-29. TED T5A-2 Self-Oscillating, DC, and Injection-Locked Operation

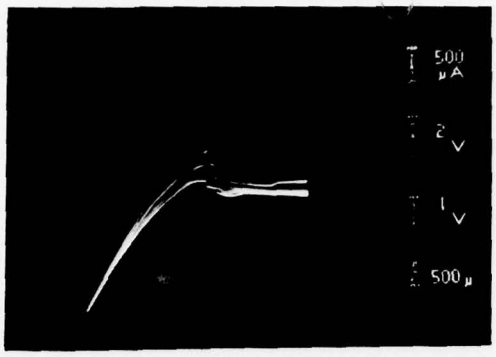
$f_{in} = 2 \times f_o$

POWER IN [dBm]	$-\Delta f_o$ [MHz]	$+\Delta f_o$ [MHz]	LOCKING BW [MHz]
-18	10	14	24
-15	18	21	39
-12	22	28	50
-9	28	39	67
-6	46	70	116
-3	40	128	168
0	46	400	446
+3	30	500	530



V_{AC}	11.4 V
V_G	-3 V
I_{AC}	7 mA
f_o	5.0 GHz

Figure 6-30. TED T5A-3 Self-Oscillating, DC, and Injection-Locked Operation



V_{AC}	11.3 V
V_G	-2.25 V
I_{AC}	2.1 mA
f_o	5.0 GHz

$f_{in} = 2 \times f_o$

POWER IN [dBm]	$-\Delta f_o$ [MHz]	$+\Delta f_o$ [MHz]	LOCKING BW [MHz]
-18	20	18	38
-15	32	54	86
-12	51	75	126
-9	75	90	165
-6	102	118	120
-3	120	180	300
0	190	340	530
+3	250	>500	>750

Figure 6-31. TED T5A-5 Self-Oscillating, DC, and Injection-Locked Operation

$f_{in} = 2 \times f_o$

POWER IN [dBm]	$-\Delta f_o$ [MHz]	$+\Delta f_o$ [MHz]	LOCKING BW [MHz]
-18	38	18	56
-15	90	32	122
-12	102	68	170
-9	111	135	246
-6	130	180	310
-3	150	>600	
-0	180	>600	
+3	180	>600	

V_{AC}	11.7 V
V_G	-2.85 V
I_{AC}	6.5 mA
f_o	5.0 GHz

Figure 6-32. TED T5A-6 Self-Oscillating, DC, and Injection-Locked Operation

6.3 INTEGRATED ANALOG MULTIPLIER

The multiplier chips are mounted on 3-port, coplanar test fixtures. DC blocks at each port are used to maintain dc isolation. Each multiplier section is biased individually to minimize the possibility of forward biasing a gate or of exceeding the maximum drain voltage of an individual device. When nominal multiplier bias conditions are obtained, the RF tests are performed.

The RF test setup is shown in Figure 6-33. The signal levels of the two inputs are measured and applied to the multiplier. The output level at the difference frequency is then measured using a spectrum analyzer. The performance of the multiplier is expressed in terms of the K factor or ratio of output to product of the input power levels. Constant K curves derived from the measurements are plotted in Figures 6-34 through 6-37.

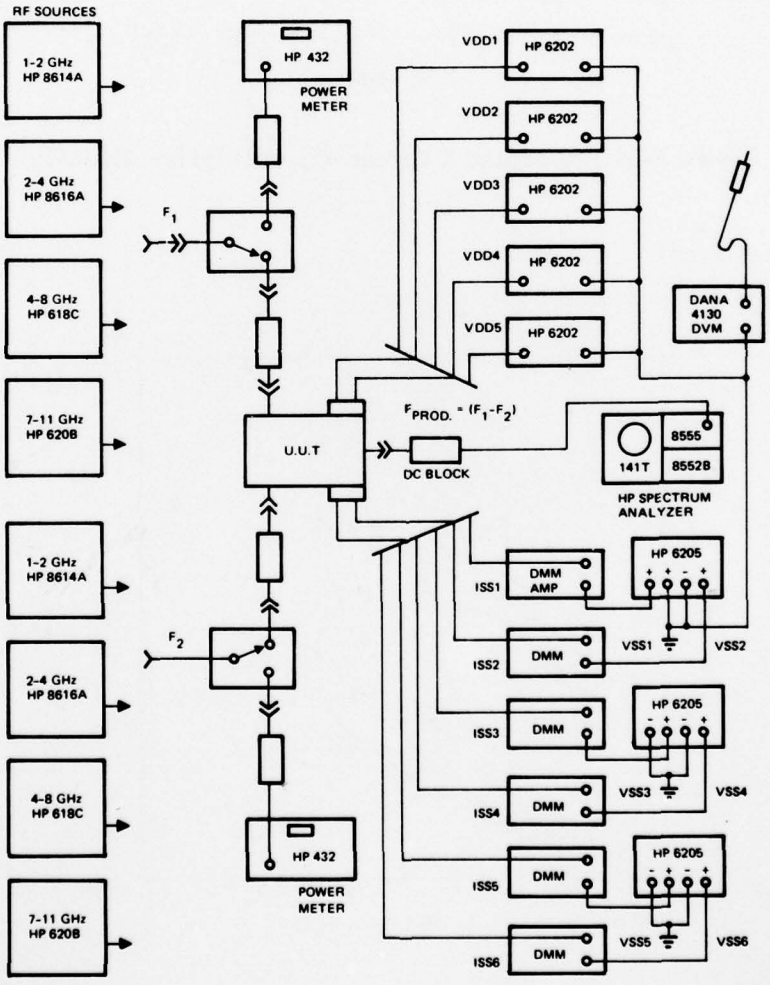


Figure 6-33. GaAs Analog Multiplier K-Factor Test Setup

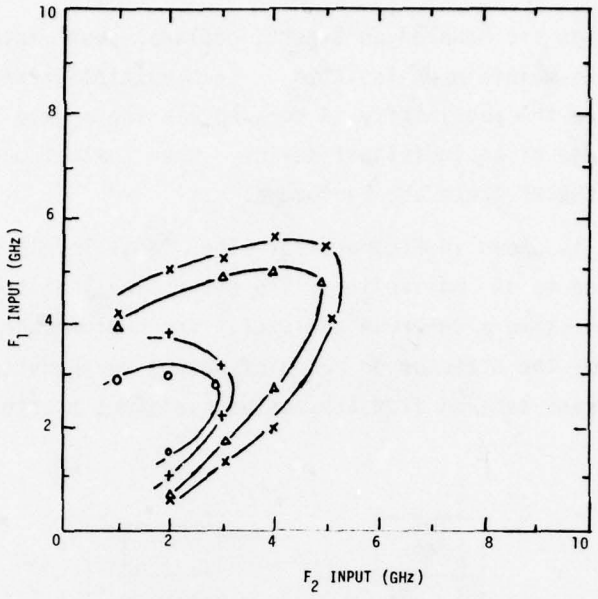


Figure 6-34. Constant K Curves for Multiplier R12-C15L

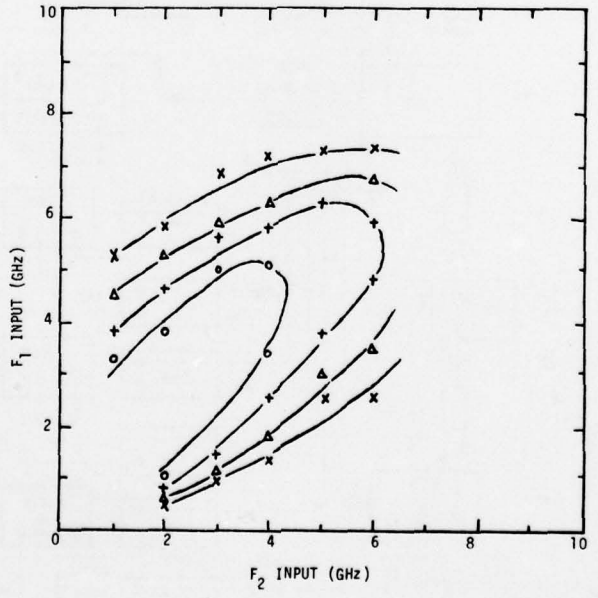


Figure 6-35. Constant K Curves for Multiplier R19-C12L

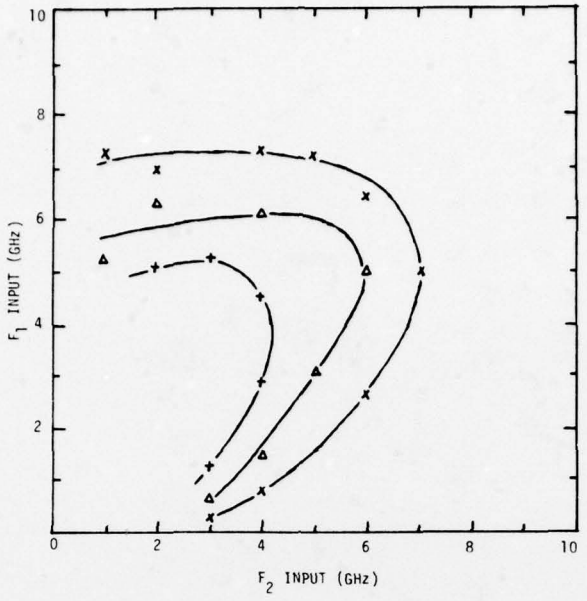


Figure 6-36. Constant K Curves for Multiplier R10-C3L

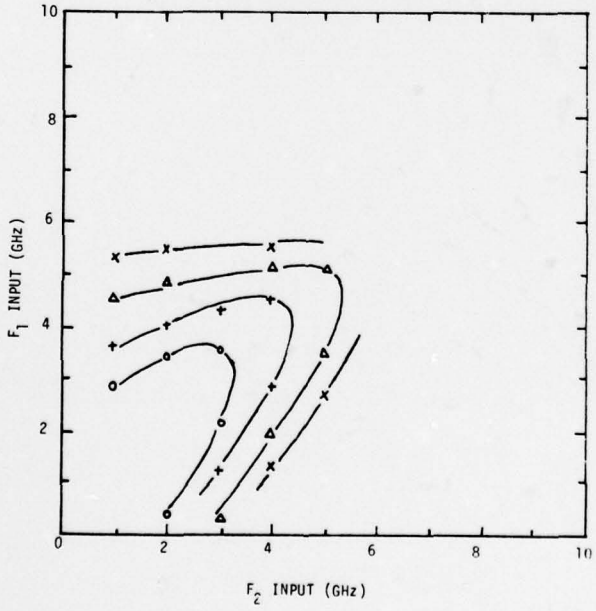


Figure 6-37. Constant K Curves for Multiplier R10-C6L